編號： 208

國立成功大學 104 學年度碩士班招生考試試題

系所組別：電機資訊學院-資訊聯招

考試科目：計算機組織與系統

考試日期：0211，節次：1

※ 考生請注意：本試題不可使用計算機。 請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

共 10 題 (4 頁)，請在答案卷作一表格如下，並清楚地填入這些題目的答案，否則不予計分。

題號	答案
1	(1) (2) (3) (4) (5)
2	(1) (2) (3) (4) (5)
3	(1) (2) (3) (4) (5)
4	(1) (2) (3) (4)
.....	....

op(31:26)

28–26 31–29	0(000)	1(001)	2(010)	3(011)	4(100)	5(101)	6(110)	7(111)
0(000)	R-format	Bltz/gez	jump	jump & link	branch eq	branch ne	blez	bgtz
1(001)	add immediate	addiu	set less than imm.	set less than imm. unsigned	andi	ori	xori	load upper immediate
2(010)	TLB	FlPt						
3(011)								
4(100)	load byte	load half	lwl	load word	load byte unsigned	load half unsigned	lwr	
5(101)	store byte	store half	swl	store word			swr	
6(110)	load linked word	lwc1						
7(111)	store cond. word	swc1						

op(31:26)=010000 (TLB), rs(25:21)

23–21 25–24	0(000)	1(001)	2(010)	3(011)	4(100)	5(101)	6(110)	7(111)
0(00)	mfc0		cfc0		mtc0		ctc0	
1(01)								
2(10)								
3(11)								

op(31:26)=000000 (R-format), funct(5:0)

2–0 5–3	0(000)	1(001)	2(010)	3(011)	4(100)	5(101)	6(110)	7(111)
0(000)	shift left logical		shift right logical	sra	sllv		srlv	srav
1(001)	jump register	jalr			syscall	break		
2(010)	mfhi	mthi	mflo	mtlo				
3(011)	mult	multu	div	divu				
4(100)	add	addu	subtract	subu	and	or	xor	not or (nor)
5(101)			set l.t.	set l.t. unsigned				
6(110)								
7(111)								

Figure 1. Tables for MIPS Instruction Encoding

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1. **[7%]** Determine whether each of the following statements is true (T) or false (F).
   (1) **[1%]** Program execution time reduces when the clock rate increases.
   (2) **[1%]** Program execution time reduces when the CPI increases.
   (3) **[1%]** Program execution time reduces when the instruction count (IC) increases.
   (4) **[2%]** Suppose the floating point instructions are enhanced and can run 10 times faster. If the execution time before the floating point enhancement is 80 seconds and three-fourth of the execution time is spent executing floating-point instructions, the overall speed up is at least 3.
   (5) **[2%]** Suppose the floating point instructions are enhanced and can run 20 times faster. If the execution time before the floating point enhancement is 80 seconds and one-half of the execution time is spent executing floating-point instruction, the overall speed up is at least 2.
2. **[7%]** Determine whether each of the following statements is true(T) or false(F)
   (1) **[1%]** R-type and I-type MIPS instruction can be distinguished by the opcode of an instruction.
   (2) **[1%]** Base addressing mode is used by I-format instructions
   (3) **[1%]** PC-relative addressing is used by J-format
   (4) **[2%]** Suppose the program counter (PC) is at address 0x0000 0000. It is possible to use one single branch-on-equal(beq) MIPS instruction to get to address 0x00030000
   (5) **[2%]** Suppose the program counter (PC) is at address 0x0000 0000, it is possible to use the jump MIPS instruction to get to 0xFFFFFFB0
3. **[6%]** The following descriptions are about IEEE 754 single precision float point format. Determine whether each of the following statements is true (T) or false (F) ?
   (1) **[1%]** The float point format has 1 sign bit, 8 exponent bits, and 23 fraction bits.
   (2) **[1%]** The smallest positive number it can represent is $0000\ 0001\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000_2$
   (3) **[1%]** The result of "Divide 0 by 0" is $0111\ 1111\ 1000\ 0000\ 0000\ 0000\ 0000\ 0000_2$
   (4) **[1%]** To improve the accuracy of the results, IEEE 754 has one extra bit for rounding.
   (5) **[2%]** 0.75_{10} is represented by $1011\ 1111\ 0100\ 0000\ 0000\ 0000\ 0000\ 0000_2$

MIPS instructions	Address	Corresponding Assembled Instruction					
Loop: sll $t1, $s3, 2	40000	0	0	19	9	4	0
(1) add $t1, $t1, $s6	40004	0	9	22	9	0	(4)
lw $t0, 0($t1)	40008	(3)	9	8	0		
bne $t0, $s5, Exit	40012	5	8	21	(1)		
addi $s3, $s3, 1	40016	8	19	19	1		
j Loop	40020	2	(2)				
Exit:	40024	.....					

4. **[10%]** Refer to the above table and Figure 1. The right side of the above table is the assembled instructions of the MIPS instructions in the left side. The starting address of the loop is 40000_{10} in memory. What are the value of (1), (2), (3) and (4)? Express your answers in decimal numbers.

5. **[15%]** Refer the following instruction sequence:

Instruction sequence
lw $1,40($2)
add $2,$3,$3
add $1,$1,$2
sw $1,20($2)

(1) **[5%]** Find all data dependences in this instruction sequence.

(2) **[5%]** Find all hazards in this instruction sequence for a 5-stage pipeline with and without forwarding.

(3) **[5%]** To reduce the clock cycle time, we are considering a split of the MEM stage into two stages. Repeat (2) for this 6-stage pipeline.

6. **[5%]** Suppose that in 1000 memory references there are 50 misses in the first-level cache, 20 misses in the second-level cache, and 5 misses in the third-level cache. Assume the miss penalty from the L3 cache to memory is 100 clock cycle, the hit time of the L3 cache is 10 clocks, the hit time of the L2 cache is 4 clocks, the hit time of L1 is 1 clock cycle. What is the average memory access time? Ignore the impact of writes.

7. **[15%]** The C-like pseudocode of two programs: *programP* and *programA* is shown below.

programP

```
main() {
    int x ;
    x = fork();
    if ( x > 0 ) {    fork();   printf("1");    }
    else if ( x == 0 ) {
        printf("2");
        fork();
        exec("programA");
        printf("3");
    }
    while (1);
}
```

programA

```
main() {
 printf("A");
 while (1);
}
```

(1) **[5%]** Please draw the parent-child process relationship graph resulting from the execution of the *programP*. Explain your answer.

(2) **[10%]** What is the output of the *program*? Explain your answer.

8. **[15%]** Assume that a process currently runs in the user mode of an x86 system. Which of the following situation(s) **always** cause a transition from the user mode to the kernel mode? (a) a timer interrupt occurs and the time quantum of the process has not expired, (b) a timer interrupt occurs and the time quantum of the process has expired, (c) TLB hits, (d) TLB misses, (e) the process executes a memory access instruction. Please briefly explain your answer.

9. **[10%]** For a memory access in a virtual memory system,

(1) **[5%]** is it possible that TLB hits and page fault occurs? Explain your answer.

(2) **[5%]** is it possible that TLB misses and page fault does not occur? Explain your answer.

10. **[10%]** Please explain why processor affinity is considered when an operating system schedules processes in a multi-processor system.