國立臺灣科技大學101學年度碩士班招生試題

系所組別： 資訊工程系碩士班

科　　目： 資訊工程概論
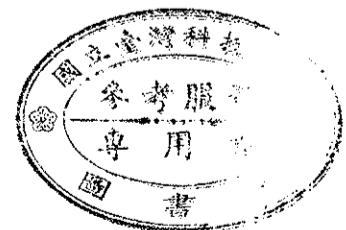
（總分為100分）

1. **(9%)** Consider the following snapshot of a system:

Resource / Process ID	Allocated				Max Required			
	A	B	C	D	A	B	C	D
1	0	0	1	4	0	6	5	6
2	0	6	3	2	0	6	5	2
3	1	3	5	4	2	3	5	6
4	1	0	0	0	1	7	5	0
5	0	0	1	2	0	0	1	2

Currently available resource [A, B, C, D] = [1, 5, 2, 0]. Will the system be in a safe state? **You must show step-by-step how you arrive at your answer to receive full credit.**

2. **(12%)** Given a disk drive with seek time 5ms per cylinder and disk request for cylinders 12, 24, 22, 4, 42, 8, and 40, in that order. For each the following algorithm, state the order in which the quests are serviced **and** compute the total seek time required. Assume that the disk arm is moved from cylinder 16 and is now at cylinder 22.

(a) **(3%)** first come first serve (FIFO)

(b) **(3%)** elevator algorithm

(c) **(3%)** shortest seek time first (SSTF)

(d) **(3%)** optimal ordering

3. **(9%)** For each of the following statements, decide TRUE or FALSE. You **MUST** justify your answer to receive full credit.

(a) **(3%)** In demand paging memory management, first-in-first-out (FIFO) paging policy usually results in lower external fragmentation comparing to most-recently-used (MRU) paging policy.

(b) **(3%)** Given a hard drive with 6000 RPM spin speed, 1 KB per sector, and 128 sectors per track, then the average latency of this hard drive is lower than 6 ms and the burst data rate is higher than 10 MB/s.

(c) **(3%)** In distributed systems, using mutex to lock shareable resources can reduce overall latency of operations.

（總分為100分）

4. **(4%)** Please compute the total number of execution for the instruction of $x++$?

```
for (i = 1; I <= n; i++)
  for (j = 1; j <= i; j++)
     for(k = 1; k <= j; k++)
        x++;
```

5. **(4%)** In C we can declare an array as follows:

int A[10][10];

if the starting address of A is α and sizeof(int) is 4 and C use Row Major Order to arrange its array please compute the address for A[6][7]

6. **(7%)** With respect to singly linked list:
   - (a) **(3%)** Give an example when stack is a better choice than a queue.
   - (b) **(4%)** You are given the head pointer to a singly linked list with a loop or cycle in it. If you follow the pointers to walk this list to find the end of the list, you will never terminate. Devise an algorithm in terms of pseudo-code to check whether the list contains a loop in $O(n)$ time and space complexity.

7. **(4%)** A binary tree has 64 nodes and what's the possible maximum height and what's the minimum height? (A tree has only a node has a height of one).

8. **(4%)** Please write the adjacent matrix for the following graph
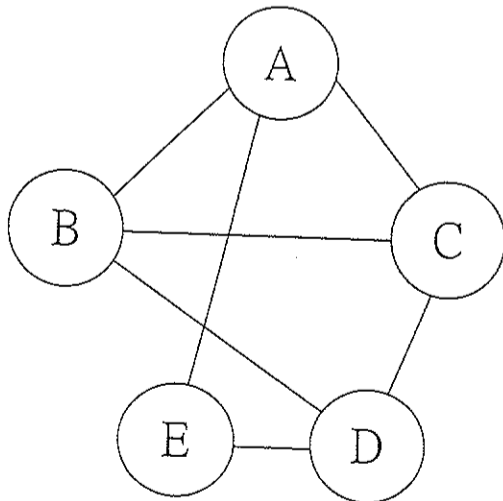
（總分為100分）

9. **(12%)**Simulate the following method
   (a) **(4%)**Draw the final result after keys 120, 310, 110, 215, 115 are inserted into a max heap sequentially
   (b) **(2%)**Draw the final result after an element is deleted from the max heap constructed in (i).
   (c) **(4%)**Draw the final result after keys 120, 310, 110, 215, 115, are inserted into a binary search tree sequentially
   (d) **(2%)**Draw the final result after 110 is deleted from the binary search tree constructed in (iii).

10. **(10%)**You are going to enhance a machine, and there are two possible implementations: either make multiply instructions run 4 times faster than before, or make memory access instructions run 2 times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 50% for memory access instructions, and 30% for other tasks.
    (a) **(3%)**What will the speedup be if you improve only multiplication?
    (b) **(3%)**What will the speedup be if you improve only memory access?
    (c) **(4%)**What will the speedup be if both implementations are made?

11. **(15%)**Assuming a cache of 4096 blocks, a four-word block size (1 word = 4 bytes), and a 32-bit address, find the total number of sets and the total number of tag bits for
    (a) **(5%)** a directed-mapped cache
    (b) **(5%)** a 4-way set-associative cache
    (c) **(5%)** a fully associative cache

12. **(10%)**Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 1GHz. Assume a main memory access time of 100ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 5%.
    (a) **(5%)**Compute the effective CPI with one level of caching

    (b) **(5%)**How much faster will the machine be if we add a secondary (L2) cache that has a 20ns access time and is large enough to reduce the miss rate to main memory to 1%?