國立臺北科技大學 101 學年度碩士班招生考試

系所組別：2230 電腦與通訊研究所丙組

第二節　電子學　試題

注意事項：

1. 本試題共 6 題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

(請依序於答案卷之答案欄內作答)

1. An amplifier exhibits two poles at 100 MHz and 10 GHz, and a zero at 1 GHz. Construct the Bode plot of $|V_{out}/V_{in}|$. (10 %)

2. We wish to design the MOS cascode of Fig. 1 for an output impedance of 200 kΩ and bias current of 0.5 mA. Assume that, for each transistor, the threshold voltage $V_{th} = 0.4$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, the channel length modulation coefficient $\lambda = 0.1\ \text{V}^{-1}$, and the transistor aspect ratio $(W/L)_1 = (W/L)_2$.

(a) Determine $(W/L)_1$. (10 %)

(b) Calculate the required value of V_{b2}. (10 %)

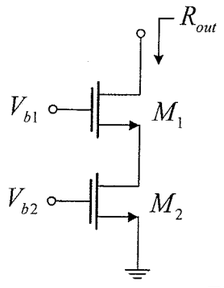

Fig. 1

3. We wish to design the MOS cascode of Fig. 2 for an input pole of 5 GHz and an output pole of 10 GHz. Assume M_1 and M_2 are identical, the overdrive voltage $(V_{GS} - V_{th})$ for each transistor is 200 mV, $I_D = 0.5$ mA, $C_{GS} = (2/3)WLC_{ox}$, $L = 0.18\ \mu$m, $C_{ox} = 12\ \text{fF}/\mu\text{m}^2$, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $\lambda = 0$, and $C_{GD} = C_0 W$, where $C_0 = 0.2\ \text{fF}/\mu\text{m}$ denotes the gate-drain capacitance per unit width.

(a) Determine the channel width W of each transistor (M_1 and M_2 are identical). (5 %)

(b) Use Miller's approximation for C_{GD2} to determine the maximum allowable values of R_G, R_D. (10 %)

(c) Determine the voltage gain. (5 %)

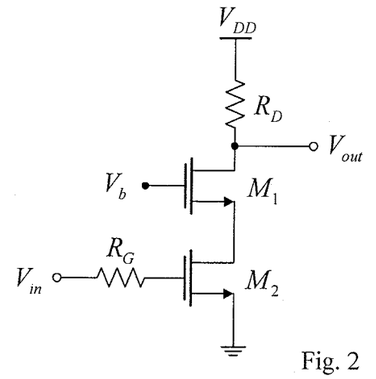

Fig. 2

4. Design a common-base stage shown with Fig. 3 for a voltage gain of 10, and an input impedance of 50 Ω. Assume $I_S = 5\times10^{-16}$ A, $V_T = 26$ mV, $V_A = \infty$, $\beta = 100$, and $V_{CC} = 2.5$ V. Besides, the resistance R_E is given as 500 Ω and the current through R_2 is 11 times of the current through the transistor base.

(a) Determine R_C, R_1, and R_2. (12 %)

(b) If this amplifier is used at the receiver front-end of a 900 MHz cell phone. Compute C_1 and C_B. (8 %)

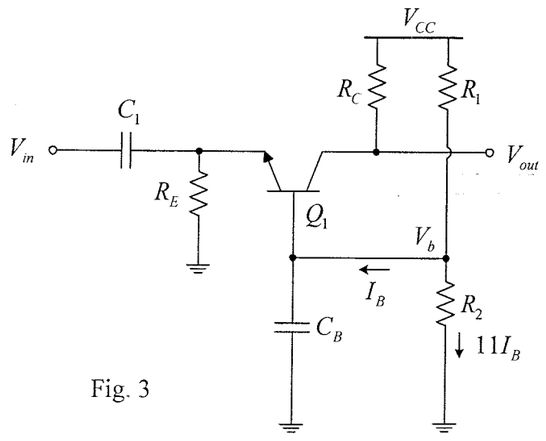

Fig. 3

注意：背面尚有試題

5. A differential amplifier is illustrated in Fig. 4. For simplicity, assume M_1 and M_2 are identical and neglect channel-length modulation in M_1 and M_2. Show the common-mode rejection ratio (CMRR) of this amplifier is

$$CMRR = \left(1 + 2g_{m1}r_{o3}\right)\frac{R_D}{\Delta R_D}$$

where g_{m1} is the transconductance of M_1 and r_{o3} is the output impedance of M_3. (15 %)

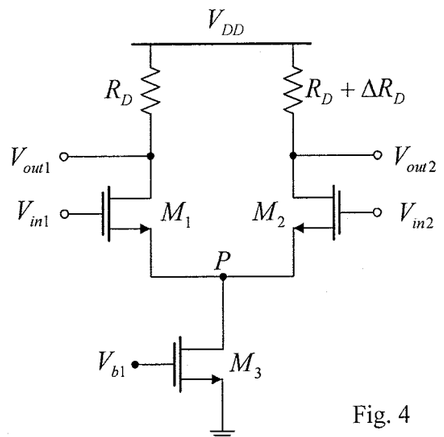

Fig. 4

6. Fig. 5 is an active filter. Assume the gain of the op-amp is very large, please:
   (a) Compute the response of the circuit, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. (5 %)
   (b) Show the Bode plot when $R_1C_1 < R_2C_2$. (5 %)
   (c) Show the Bode plot when $R_1C_1 > R_2C_2$. (5 %)

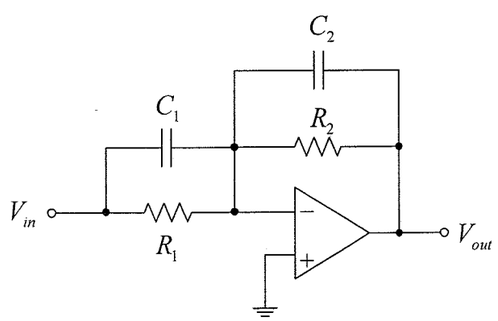

Fig. 5