國立雲林科技大學
101學年度碩士班暨碩士在職專班招生考試試題

系所：電子光電所
科目：計算機組織(1)

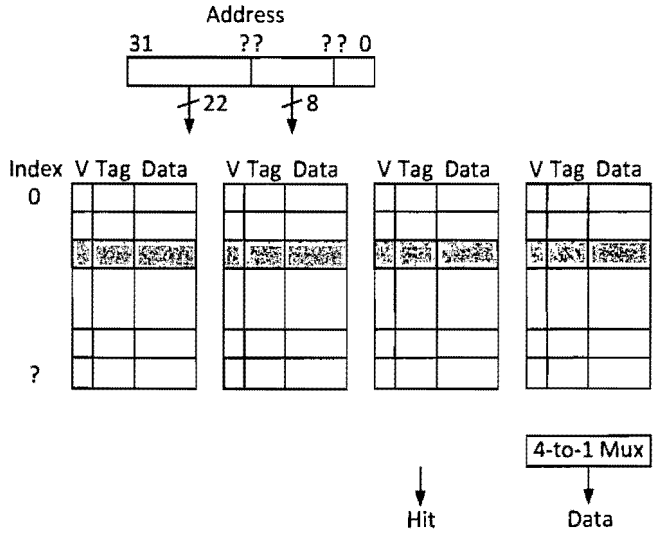
1. Number system conversion (10%)
   (a) Binary to octal number : $(10010001101011.110100000110)_2 = (\ ?\ )_8$
   (b) Hexadecimal to binary number : $(316.C)_{16} = (\ ?\ )_2$
   (c) Please find the 1's complement of $(1001000)_2 = (\ ?\ )$
   (d) Please find the 10's complement of $(243700)_{10} = (\ ?\ )$
   (e) Binary number to Gray Code: $(1011001)_2 = (?)$

2. Explain the following abbreviations. (10%)
   (a) RISC (3%)
   (b) CISC (3%)
   (c) VLIW (2%)
   (d) SIMD (2%)

3. Design and draw the schematic of a 4-bit carry lookahead adder. (10%)

4. Trace the Booth's algorithm step b y step for the multiplication of 3x(-6). (10%)

5. Complete the following figure for implementation of a four-way set-associative cache with four comparators and a 4-to-1 multiplexor. (10%)



6. Given the memory values below and a one address machine with an accumulator, what values do the following instructions load into the accumulator? (10%)
   - Memory word 20 contains 40
   - Memory word 30 contains 50

- Memory word 40 contains 60
- Memory word 50 contains 70.

(a) LOAD IMMEDIATE 20
(b) LOAD DIRECT 20
(c) LOAD INDIRECT 20
(d) LOAD IMMEDIATE 30
(e) LOAD DIRECT 30
(f) LOAD INDIRECT 30

7. For the 16 bit binary number 1001 0101 1100 0011, show the effect of (10%)
   (a) A right shift of 4 bits with zero fill
   (b) A right shift of 4 bits with sign extension
   (c) A left shift of 4 bits
   (d) A left rotate of 4 bits
   (e) A right rotate of 4 bits.

8. Consider each instruction has 5 stages in a computer with pipelining techniques. Each stage takes 4ns. (10%)
   (A) What is the maximum number of MIPS that this machine is capable of with 5-stage pipelining techniques?
   (B) What is the maximum number of MIPS that this machine is capable of in the absence of pipelining?
   (C) From the above questions (A) and (B), we can know that the pipelining allows a tradeoff between latency and processor bandwidth. Please explain what is latency and what is bandwidth?

9. There are two computers A and B with the following performance information. (10%)
   Computer A: Cycle time = 250 ps, Cycle per instruction = 2.0
   Computer B: Cycle time = 600 ps, CyclE per instruction = 1.2
   If both computers have the same instruction set architecture, which computer is faster? How many times is one faster as the other?

10. Computer A has 2GHz clock. It takes 10s CPU time to finish one given task. We want to design Computer B to finish the same task within 5s CPU time. The clock cycle number for Computer B is 2 times that of Computer A. So, what clock rate should be designed for Computer B? (10%)