國立雲林科技大學
101 學年度碩士班暨碩士在職專班招生考試試題

系所：資工系
科目：計算機組織(2)

1. You are going to enhance a machine, and there are two possible improvements: either makes multiply instructions run five times faster than before, or make memory access instructions run two times faster than before. You repeatedly run a program that takes 10 seconds to execute. Of this time, 25% is used for multiplication, 50% for memory access instructions, and 25% for other tasks.
   - What will the speedup be if you improve only multiplication? (6%)
   - What will the speedup be if you improve only memory access? (6%)
   - What will the speedup be if both improvements are made? (6%)

2. A CPU designs with pipeline technique. For pipelined execution, assume that half of the load instructions incur the data hazards (required one clock stall), that the one-quarter of the branches have control hazards (required one clock for branch delay). If one program has 40% loads, 15% stores, 20% branches, 5% jumps, and 20% ALU. What is the average CPI? (14%)

3. Table 1 shows the CPI values for different instruction classes. There are two compilers which compile the same program. Table 2 shows the results for each compiler.

Table 1

instruction class	CPI
A	1
B	4
C	2

Table 2

Code from	Instruction counts (**in millions**) for each instruction class		
	A	B	C
Compiler 1	6	1	1
Compiler 2	10	1	1

If the machine's working frequency is 100MHz，please answer the following question.

(a) What is the MIPS value for compiler 1 and compiler 2? (6%)
(b) What is the CPI value for compiler 1 and compiler 2 ?(6%)
(c) What is the CPU time for compiler 1 and compiler 2 ?(6%)

4. Show the IEEE 754 binary representation of the number of -0.75_{ten} in single precision. (10%)

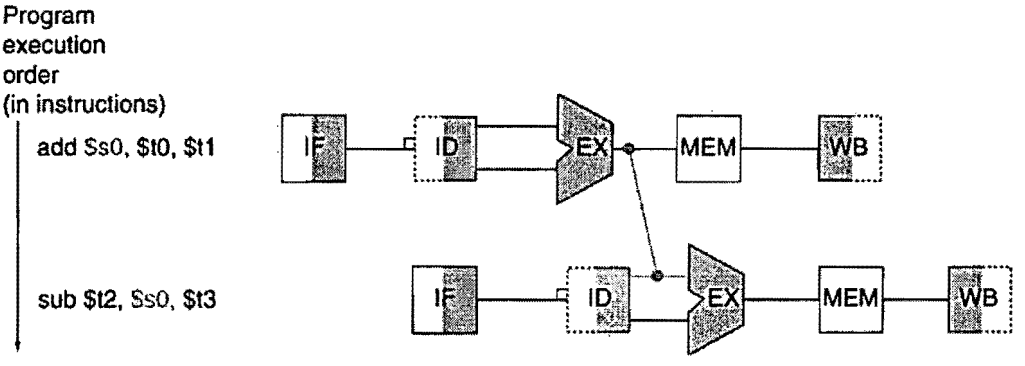
5. How many total bits are required for a directed-mapped cache with 16KB of data and 4-word blocks, assuming a 32-bit address? (10%)

6. Consider a cache with 64 blocks and a block size of 16 bytes. To what block number does byte address 1200 map? (10%)

國立雲林科技大學
101 學年度碩士班暨碩士在職專班招生考試試題

系所：資工系
科目：計算機組織(2)

7. For the instruction `sub $t2, $s0, $t3`, how many clock cycles should it have to waste after a forwarding path (shown in the figure) is added? (10%)



8

I-MEM	Add	Mux	ALU	Regs	D-Mem	Sign-extend	Shift-left-2
400ps	100ps	30ps	120ps	200ps	350ps	20ps	0ps

(a)What is the clock cycle if the only type of instructions we need to support are ALU instructions (`add`, `and`, etc.)? (5%)

(b)What is the clock cycle time if we only had to support `lw` instructions? (5%)