國立高雄應用科技大學
101 學年度碩士班招生考試
光電與通訊工程研究所

准考證號碼□□□□□□□□□□ （考生必須填寫）

電子學

試題　共 4 頁第 1 頁

注意：a. 本試題共 5 題、每題 20 分，共 100 分。

b. 作答時不必抄題，但必須書寫計算過程否則不予計分。

c. 考生作答前請詳閱答案卷之考生注意事項，各試題答案必須依題號順序寫在試卷指定的答案欄；寫錯位置不予計分。

1. For the circuit shown in Fig. 1, derive the transfer function $T(s) = V_O(s)/V_i(s)$. For R_1 = 10 kΩ, R_2 = 40 kΩ, and C = 0.1 μF, find the 3-dB frequency f_o. (20%)

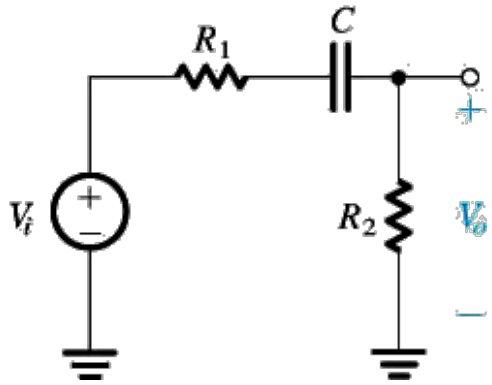

Fig. 1

2. Design the circuit shown in Fig. 2 to have an input resistance of 100 kΩ and a gain that can be varied from -1 V/V to -10 V/V using the 10 kΩ potentiometer R_4. What voltage gain results when the potentiometer is set exactly at its middle value? (20%)

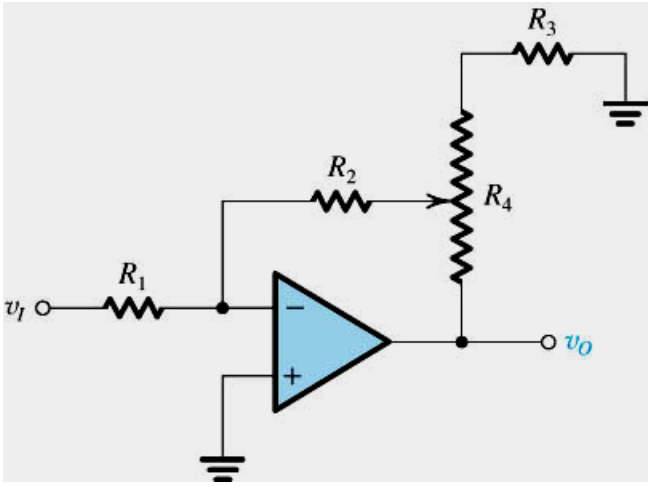

Fig. 2

3. Consider the half-wave rectifier circuit of Fig. 3 with the diode reversed. Let v_S be a sinusoid with 15 V peak amplitude, and let R = 1.5 kΩ. Use the constant-voltage-drop diode model with V_D = 0.7 V. (a) Sketch the transfer characteristic. (b) Sketch the waveform of v_O. (20%)

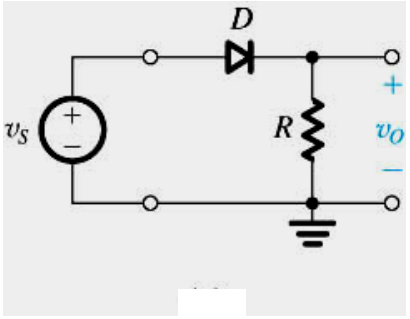

Fig. 3

4. For the circuit shown in Fig. 4, find the labeled node voltages V_1 and V_2. The NMOS transistors have V_t = 1 V, $k_n' W/L$ = 2 mA/V^2, and $\lambda = 0$. (20%)

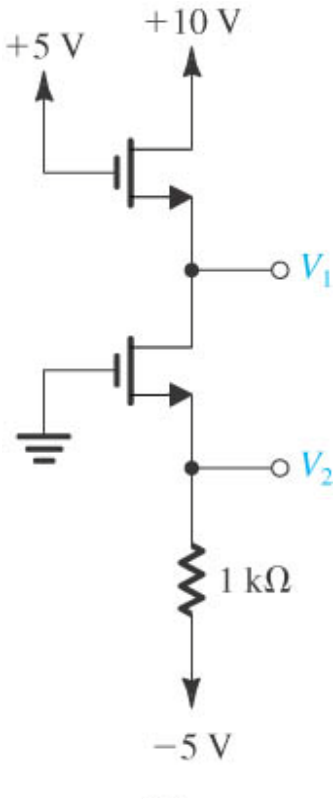

Fig. 4

5. Find the voltages at nodes V_A, V_B, V_C, and V_D in the circuit of Fig. 5. Assume $|V_{BE}|$ = 0.7 V and $\beta = \infty$. (20%)

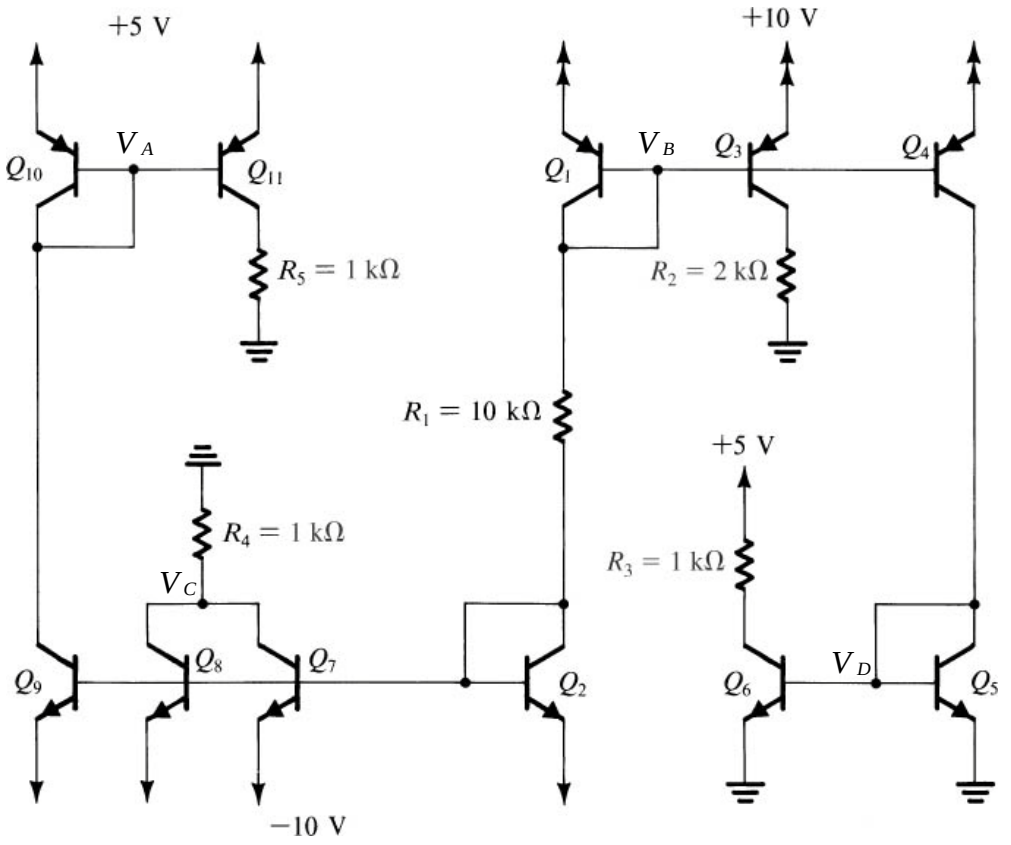

Fig. 5