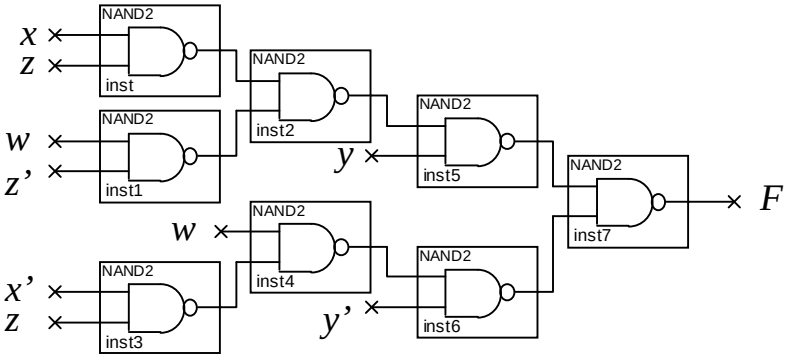
國立彰化師範大學 101 學年度碩士班招生考試試題

系所： 電子工程學系　　組別： 乙組　　科目： 計算機組織

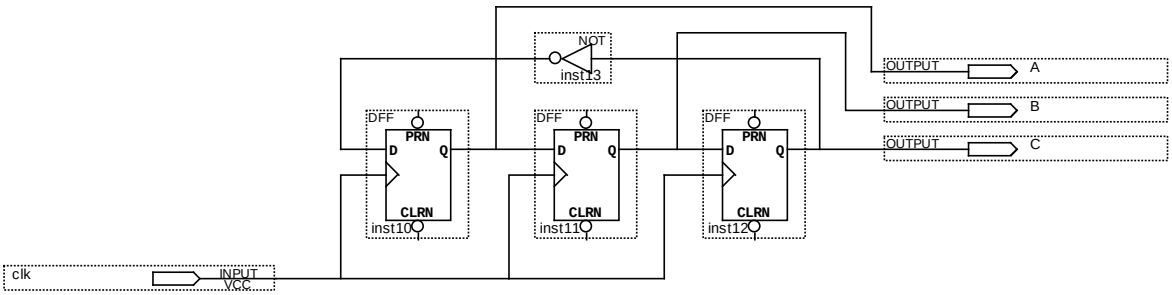
☆☆請在答案卷上作答☆☆　　

1. (a) Convert the following expression to sum of products form: (5%)
   $(a + b + c + d')(b + c' + d)(a + c)$
   (b) Convert the following expression to product of sums form: (5%)
   $bc'd + a'b'd + b'cd'$
2. Find a minimum two-level circuit for the following function sets. (10%)
   $F(A, B, C, D)=\Sigma_m(0, 2, 3, 4, 6, 7, 10, 11)$
   $G(A, B, C, D)=\Sigma_m(0, 4, 8, 9, 10, 11, 12, 13)$

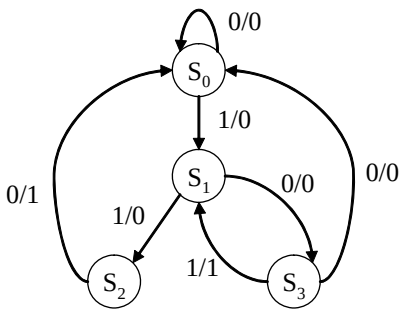
3. (a) Find an algebraic expression for the following circuit. (5%)



   (b) Derive the state table and state diagram of the following circuit. (5%)



4. Referring to the state diagram and state assignment in following figures to design the sequential logic circuit using JK-type flip-flops. (10%)



State Assignment

S	A	B
S_0	0	0
S_1	0	1
S_2	1	0
S_3	1	1

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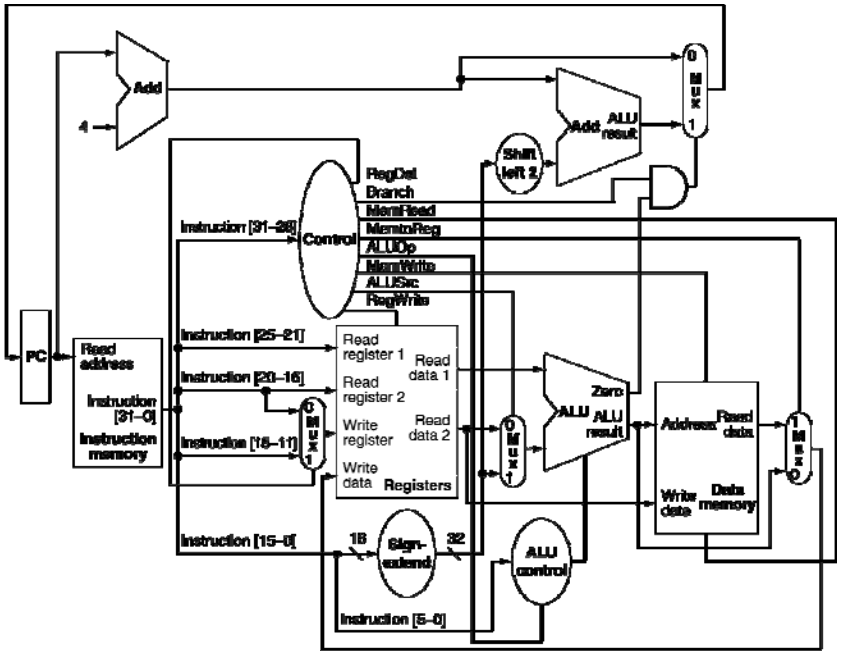
5. Using a truth table (or compact canonical forms) to demonstrate whether or not the following functions are equal: (10%)
   $f(x, y, z) = x'y' + x'z' + xy$ and $g(x, y, z) = (x + y' + z')(x' + y)$

6. The datapath of the MIPS processor is shown below. Assign appropriate value ('1', '0', 'x'(don't care)) to the control signals (RegDst, ALUsrc, MemtoReg, RegWrite, MemRead, MemWrite) when MIPS processor is executing (a) an ADD instruction, (b) a LW (Load Word) instruction, (c) a SW (Store Word) instruction, and (d) a BEQ (Branch if Equal) instruction. (20%)



control signal	ADD	LW	SW	BEQ
RegDst				
ALUSrc				
MemtoReg				x
RegWrite				0
MemRead				0
MemWrite				0

7. Translate the following C code segment into MIPS assembly code. (10%)

```
while ( j < k)
    {
        if(A[j]>=0)
            sum = sum + A[j];
        else
            sum = sum - A[j];
        j=j+1;
    }
```

   Assume that variable *j* is assigned to *R1*, variable *k* is assigned to *R2*, and variable *sum* is assigned to *R3*; the start address of integer array *A* is already stored in *R4*.

8. Explain the following terms in detail. (20%)
   (a) RAW (Read After Write) dependency and WAR (Write After Read) dependency.
   (b) Write Back cache and Write Through cache.
   (c) Virtual Memory, Page table, and TLB (Translation Look-aside Buffer).
   (d) RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer).