國立高雄師範大學 101 學年度碩士班招生考試試題

系所別：電子工程學系

科　目：電子學

※注意：1. 作答時請將試題題號及答案依序寫在答案卷上，於本試題上作答者，不予計分。
2. 請以藍、黑色鋼筆或原子筆作答，以鉛筆或其他顏色作答之部份，該題不予計分。

1. Si and GaAs are generally used in IC and photonic applications, respectively. Please explain the reasons in detail.（10%）

2. Determine and plot $v_0(t)$ for the network in Fig.1.（10%）

3. In Fig. 2, find V_{CE} and I_E.（15%）

4. The NMOS transistors in Fig.3 have $V_t = 1V$ and $k_n'W/L = 2mA/V^2$. Assume $\lambda = 0$. Determine the node voltages V_1, V_2 and V_3.（15%）

5. Consider the bias circuit of Fig. 4 for the case: $(W/L)_8=(W/L)_9=(W/L)_{10}=(W/L)_{11}=(W/L)_{13}=20$ and $(W/L)_{12}=80$.
   (a) Find the value of R_B that results in a bias current $I_B=10$ μA.（5%）
   (b) Also in a process technology having $\mu_n C_{ox}=90$ μA/V^2, find the transconductance g_{m12}.（5%）

6. For the circuit of Fig. 5, let the op amp have open-loop gain $\mu=10^4$ V/V, $R_{id}=100$ kΩ, and $r_o=1$ kΩ.
   (a) Find the voltage gain V_o/V_s.（5%）
   (b) Find the input resistor R_{in}.（5%）
   (c) Find the output resistor R_{out}.（5%）

7. For particular design of the folded-cascode op amp of Fig. 6, ±1.65 V supplies are utilized and all transistors are operated at overdrive voltages of 0.3 V magnitude. The fabrication process employed provides $V_{tn}=|V_{tp}|=0.5$ V.
   (a) Find the input common-mode range.（5%）
   (b) Find the range allowed for v_o.（5%）

8. (a) Sketch a two-input CMOS NAND gate.（6%）
   (b) Assume that for the basic inverter n=1.5 and p=5 and that the channel length is 0.25 μm, find the W/L ratios for all transistors, such that the worst-case t_{PHL} and t_{PLH} of the gate are equal to those of the basic inverter.（4%）

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9. Using the circuit of Fig. 7 design a monosatble circuit with CMOS logic for which R_{on}=100 Ω, V_{DD}=5 V, and V_{th}=0.4 V_{DD}. Use C=1 μF to generator an output pulse of duration T=1 s. What value of R should be used?（5%）

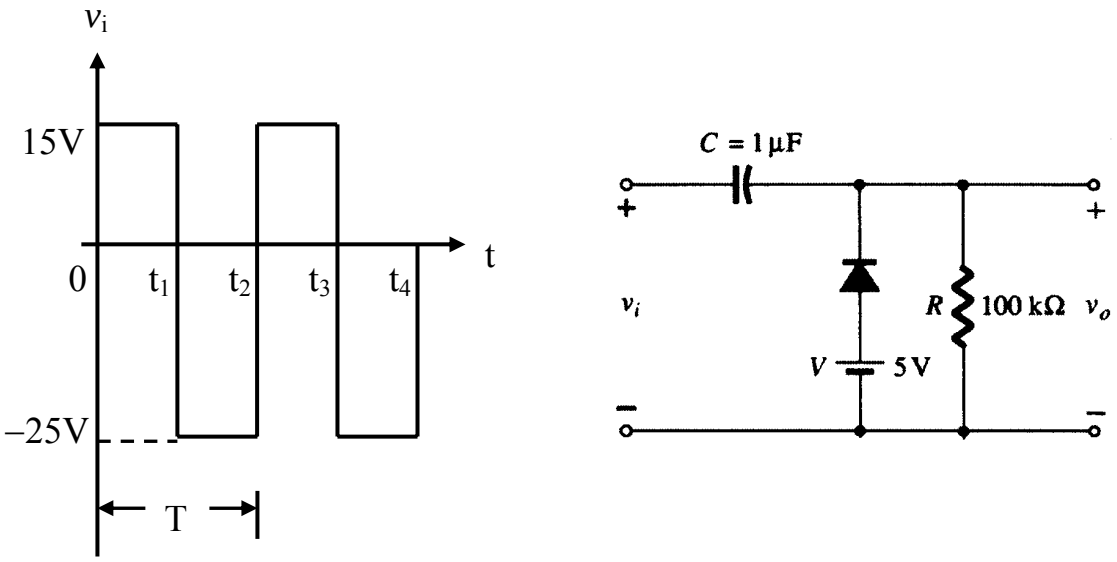

Fig. 1

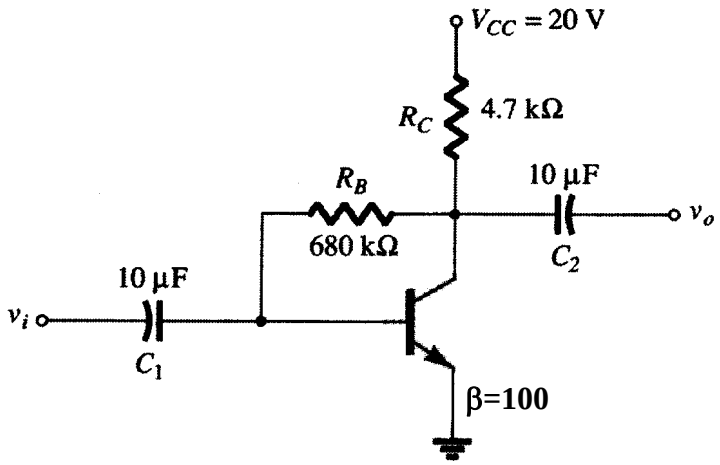

Fig. 2

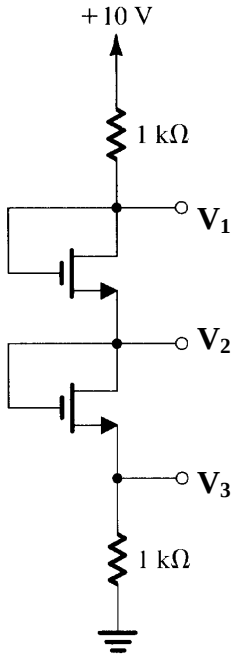

Fig. 3

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科　目：電子學

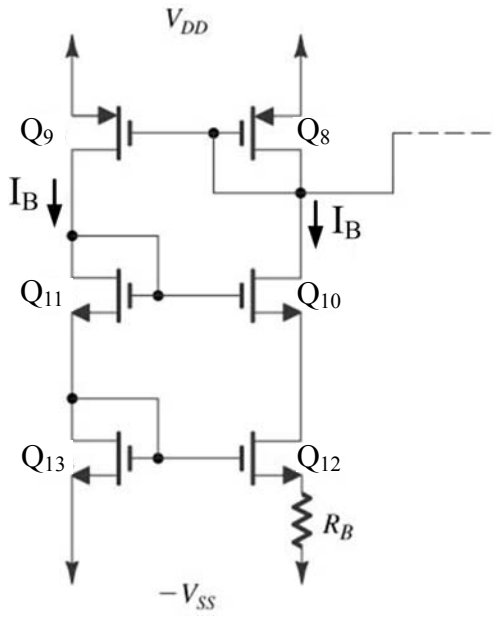

Fig. 4

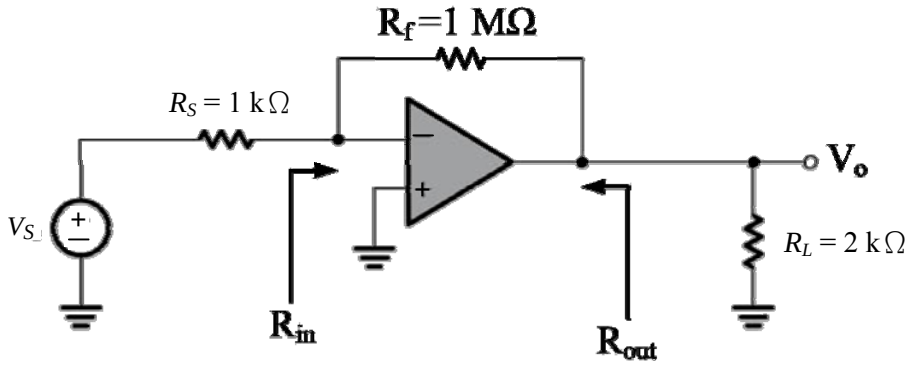

Fig. 5

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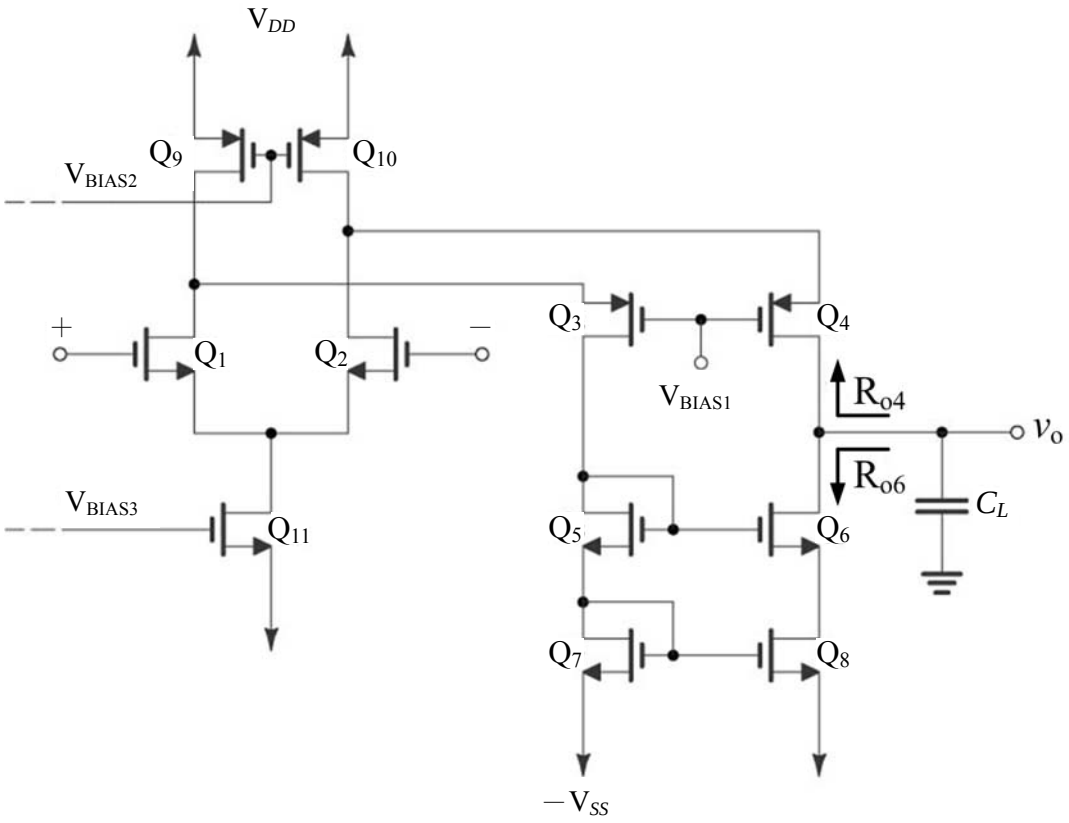

Fig. 6

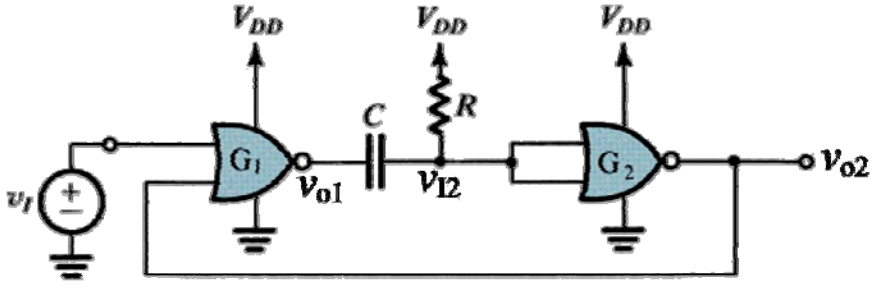

Fig. 7