

# 國立臺灣師範大學 101 學年度碩士班招生考試試題

科目：計算機系統

適用系所：資訊工程學系

注意：1.本試題共 4 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則依規定扣 pts。

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1. (10 pts)

Consider two processors (CPU A and CPU B) having the same instruction set architecture. These two processors execute the same program consisting of 1000 instructions. CPU A has a clock cycle time of 0.5ns, and a CPI (clock cycles per instruction) of 2.0 for the program. CPU B has a clock cycle time of 1.0ns, and a CPI of 1.5 for the same program.

- (a) (3 pts) Find the clock rate of CPU A (in GHz).
- (b) (3 pts) Determine the CPU time of CPU A (in ns).
- (c) (2 pts) Determine the CPU time of CPU B (in ns).
- (d) (2 pts) Suppose we want to change the clock rate of CPU B so that both CPU A and CPU B have the same CPU time for the program. Find the new clock rate of CPU B (in GHz).

2. (20 pts)

Consider a five-stage (IF, ID, EX, MEM and WB) MIPS pipeline processor **with hazard detection and data forwarding units**. Assume the processor includes separate instruction and data memories so that the structural hazard for memory references can be avoided.

- (a) (10 pts) Suppose the following code sequence is executed on the processor. Identify all the data hazards which can be solved by forwarding. Determine the total number of clock cycles required for the execution of the code sequence.

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SUB R1, R2, R3;             $R1 \leftarrow R2 - R3$   
ADD R4, R1, R6;             $R4 \leftarrow R1 + R6$   
SW R4, 12(R6);             $MEM[12 + R6] \leftarrow R4$

(b)(10 pts) Repeat part (a) for the following code sequence.

LW R5, 12(R7);             $R5 \leftarrow MEM[R7 + 12]$   
ADD R1, R2, R5;             $R1 \leftarrow R2 + R5$   
SUB R4, R1, R6;             $R4 \leftarrow R1 - R6$

3. (10 pts)

Consider a five-stage (IF, ID, EX, MEM and WB) MIPS pipeline processor with separate instruction and data memories. Suppose the following code sequence is executed on the processor.

LW R2, 16(R1);             $R2 \leftarrow MEM[R1 + 16]$   
LW R4, 20(R3);             $R4 \leftarrow MEM[R3 + 20]$   
ADD R6, R2, R4;             $R6 \leftarrow R2 + R4$   
SUB R8, R12, R4;             $R8 \leftarrow R12 - R4$   
ADD R10, R2, R8;             $R10 \leftarrow R2 - R8$   
LW R9, 20(R1);             $R9 \leftarrow MEM[R1 + 20]$   
LW R11, 24(R3);             $R11 \leftarrow MEM[R3 + 24]$

(a) (5 pts) Determine total number of memory accesses.

(b) (3 pts) Suppose there is only one miss in the instruction memory for the code sequence. Compute the miss rate of the instruction memory.

(c) (2 pts) Suppose there are two misses in the data memory for the code sequence. Compute the miss rate of the data memory.

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4. (10 pts) Consider a direct mapped cache with 64 blocks and a block size of 32 bytes.
  - (a) (3 pts) What cache block number does byte address 1600 map to?
  - (b) (3 pts) What cache block number does byte address 3209 map to?
  - (c) (2 pts) Suppose the miss rate for accessing the cache is 0.05 misses per memory access. Assume the hit time is 1 clock cycle, and the miss penalty is 100 clock cycles. What is the average memory access time (AMAT) of the cache (in clock cycles)?
  - (d) (2 pts) Suppose there are 200 memory accesses to the cache. Find the total number of memory-stall cycles.
5. (5 pts) Show the storage-device hierarchy of the contemporary computer system.
6. (5 pts) (a) What are the differences between multiprogramming and multi-tasking systems? (b) Since the operating system and the users share the hardware and software resources of the computer system, we need to make sure that an error in a user program could cause problems only for the one program that was running. For example, if a process gets stuck in an infinite loop, this loop could prevent the correct operation of many other processes. Can the multiprogramming and multi-tasking systems solve the above problem?
7. (5 pts) Explain the following terms: (a) Dual mode operation. (b) Privileged instructions. (c) Software interrupt. (d) System call. (e) PCB.
8. (5 pts) (a) What are the differences between synchronous and asynchronous I/O? (b) How do we make interprocess communication between processes which belong to different users? Note that these processes are located in a single computer system. Please state in details how the sender find the receiver.
9. (5 pts) Why the dynamically loadable kernel module is very popular in the contemporary operating systems?

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10. (5 pts) When will device drivers be invoking?
11. (5 pts) Give a situation that priority scheduling algorithm results in starvation.
12. (5 pts) Assume that S1, S2, and S3 are three statements of three different processes. How do you use the wait and signal operations of semaphore to have S1 be executed before S2 and S2 be executed before S3?
13. (5 pts) (a) Give a diagram to show the operation of inverted page table. (b) What is the advantage of inverted page table? (c) What are the disadvantages of inverted page table?
14. (5 pts) Typically, the operating system uses two levels of internal tables: a per-process open file table and a system-wide open file table. Which of the following components are stored in the per-process open file table? (註：此題為多選題)

- [A] File pointer
- [B] File-open count
- [C] Disk location of the file
- [D] Access rights during the open session
- [E] Access permission of the file
- [F] Memory Cache of the file