招生學年度	101	招生類別	碩士班
系所班別	電機工程學系 電子工程碩士班、光電工程學系碩士班(乙組)		
科目	電子學		
注意事項	本考科可使用掌上型計算機		

1. (4%) What are intrinsic and extrinsic semiconductors?

2. (10%) (a) Sketch the minority carrier distribution of a uniformly doped $n^{++}p^{+}n$ BJT operated in the active mode. (b) Explain the base width modulation effect (Early effect) of the BJT.

3. (6%) For the circuit shown in Fig.1, determine the voltages at all nodes (V_B, V_C, and V_E) and the currents in all branches (I_B, I_C, and I_E). Assume $\beta = 100$, and $V_{BE} = 0.7$ V.

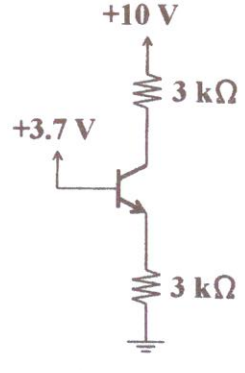

Fig.1

4. (4%) With the knowledge that $\mu_p = 0.4\ \mu_n$, what must be the relative width of n-channel and

p-channel devices if they are to have equal drain currents when operated in the saturation mode with overdrive voltages of the same magnitude?

5. (6%) Consider an NMOS with $k_n' = 100\ \mu A/V^2$, $V_t = 0.8$ V, and $W/L = 10$. Find the drain currents in the following cases.
   (a) $V_{GS} = 2$ V and $V_{DS} = 4$ V.
   (b) $V_{GS} = 4$ V and $V_{DS} = 2$ V.

6. (20%) Fig.2 shows a CS amplifier. Answer the following questions.
   (a) If the transistor has $V_t = 1$ V, and $k_n'(W/L) = 2\ mA/V^2$, find V_{GS}, I_D, and V_D.
   (b) Find g_m and r_o if $V_A = 100$ V.
   (c) Draw a complete small-signal equivalent circuit.
   (d) Find R_{in} and v_o/v_{sig}.

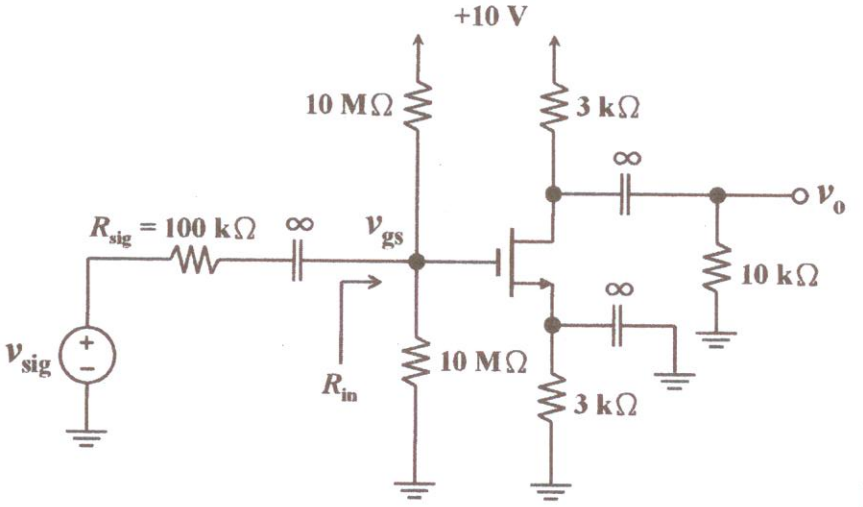

Fig.2

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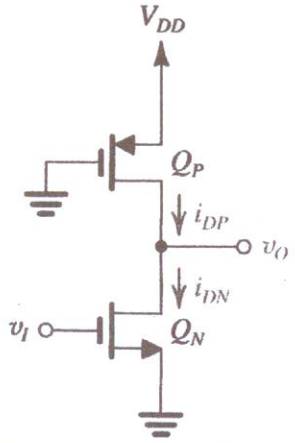
7. (15%) Consider a pseudo-NMOS inverter in Fig.3 fabricated in a 0.25μm CMOS technology for which $\mu_n C_{ox}=115\mu A/V^2$, $\mu_p C_{ox}=30\mu A/V^2$, $V_{tn}= -V_{tp}=0.5V$, and $V_{DD}=2.5V$. Let the W/L ratio of Q_N be (0.375μm/0.25μm) and r=9. Assuming a total capacitance at the inverter output of 7fF, please find:

(a) NM_H and NM_L

(b) t_{PLH} and t_{PHL}



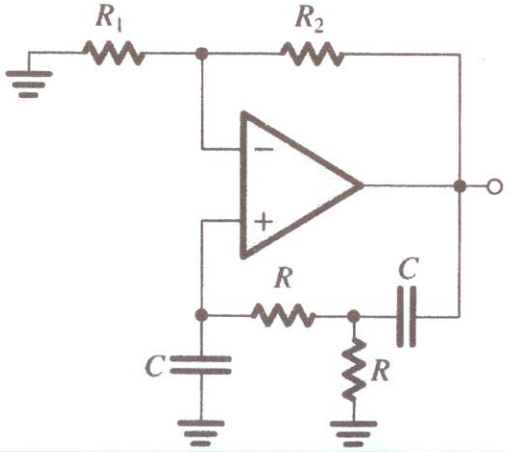


Fig.3 Fig.4

8. (10%) The Wein-Bridge oscillator is shown in Fig.4. $R=R_1=10k\Omega$ and $C=10nF$. Please determine the oscillation frequency and R_2 for oscillation.

9. (10%) Design a pseudo-NMOS logic gate circuit which performs the function of $Y = \overline{A+B+C}$.

10. (15%) Consider a source follower in Fig.5, NMOS transistor is designed with $g_m=1mA/V$ and $r_o=150k\Omega$. C_{c1} and C_{c2} are coupling capacitors. Let $R_{sig}=1M\Omega$, $R_G=4.7M\Omega$ and $R_L=15k\Omega$.
    (a) Find R_{in}, R_o, and $Av= v_o/v_i$.
    (b) Find the overall small-signal gain $G_v=v_o/v_{sig}$.

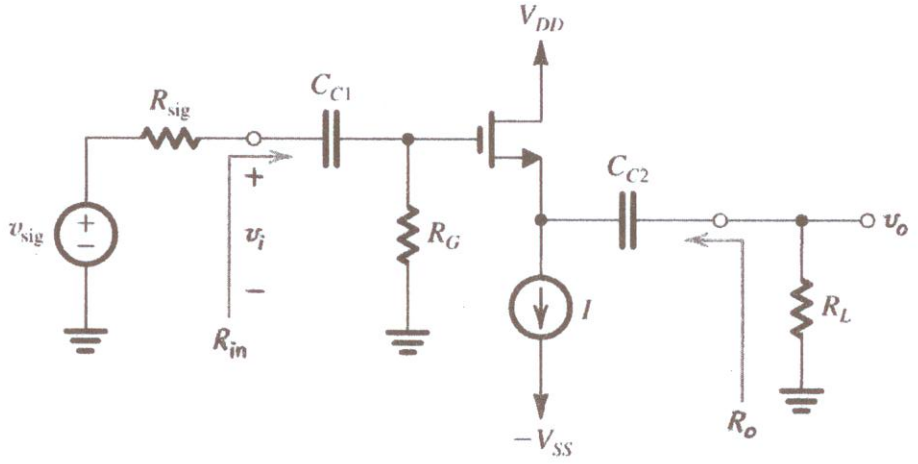


Fig.5