逢甲大學101學年度碩士班招生考試試題 編號：070 科目代碼：

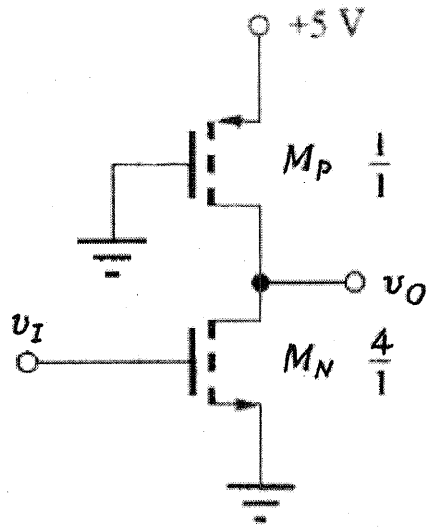
科目	數位電路(含邏輯設計)	適用系所	電子工程學系電路與系統組	時間	100 分鐘

※請務必在答案卷作答區內作答。

1a. (15%)

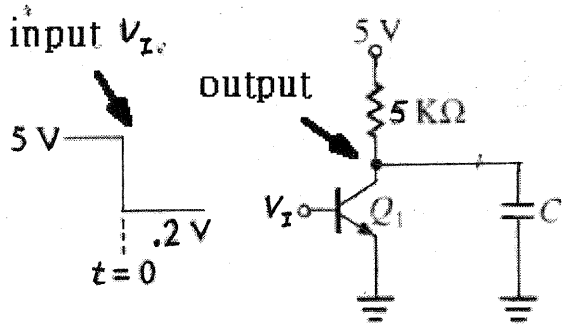
Use $\mu_n C_{ox} = 25\mu A/V^2$, $\mu_p C_{ox} = 10\mu A/V^2$, V_{TN}=1V and V_{TP}=-1V.

Find V_{OH} and V_{OL} for the following CMOS gate.



1b. (10%)

Determine the output rise time for the following circuit with C=1 pF.



2. (25%)

Use V_{DD}=3.3V, $\mu_n C_{ox} = 25\mu A/V^2$, $\mu_p C_{ox} = 10\mu A/V^2$, V_{TN}=0.75V and V_{TP}= -0.75V.

Find the noise margins NM_H and NM_L for a CMOS inverter having $(W/L)_N=(W/L)_P$.

3. (1) 5% Please **minimize** the following expression:
$\overline{C}\overline{D} + \overline{B}CD + \overline{A}C\overline{D} + AC\overline{D}$

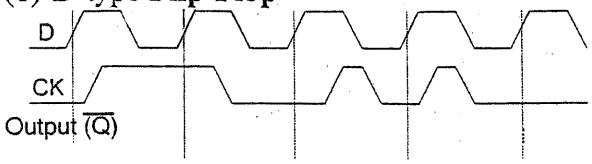
(2) 5%Please design and make the logic circuit **as simple as possible** of Y(A, B, C, D)=Σm(0,1,2,3,12,13,14,15).

4. (1) 5%Please design a **logic gate** circuit, to implement a **De-Multiplexer** for the function of 1-2 (1-input and 2-output).

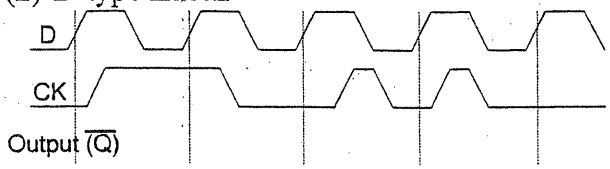
(2) 5%Please design a **concept logic circuit (block diagram only)**, to implement a **Decoder** for the function of 3-8 (3-input and 8-output) by using two 2-4 (2-input and 4-output) **Decoders**.

5. 10%Please draw the **output waveforms** for the follows logic device for $\overline{Q}$

(1) D-type **Flip-Flop**



(2) D-type **Latch**



6. (1) 10%Please use the **JK-FF** to design a **Synchronous counter** with the counting sequence of 0->1->2->3->4->5->6->7->0….. (repeat)

(2) 10%Please use the **D-FF** to design a **Asynchronous counter** with the counting sequence of 0->7->6->5->4->3->2->1->0…. (repeat)