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1. Explain the clock skew and how to alleviate it. (10%)

2. How to define the active component and the passive component? (10%)

3. Give two different static CMOS logic realizations of the Exclusive OR (XOR) function $Y = A\overline{B} + \overline{A}B$ in which the pull-down network (PDN) and the pull-up network (PUN) are dual network. (15%)

4. For a static CMOS inverter having $k_n = k_p = 100\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.8V$, $V_{DD} = 3.3$ V, and $\lambda_n = \lambda_p = 0.03\ V^{-1}$, find
   (a) Input low and high voltages: V_{IL}, V_{IH}, (5%)
   (b) Output low and high voltages: V_{OL}, V_{OH}, (5%) and
   (c) Noise margins: NM_L, NM_H. (5%)

5. As depicted in Fig. 1, assume $\lambda \neq 0$ and the transconductances of transistors M_1 and M_2 are g_{m1} and g_{m2}, respectively. If all of the transistors are operated in saturation region, please derive the
   (a) Input impedance (5%)
   (b) Output impedance (5%)
   (c) Voltage gain (5%)
   (d) At high frequency, please derive the capacitance at V_{IN} (5%)
   (e) At high frequency, please derive the capacitance at V_{OUT} (5%)

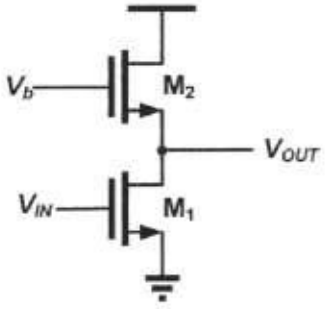

Fig. 1

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6. As depicted in Fig. 2, assume $\lambda=0$ and transconductances of transistors M_1 and M_2 are g_{m1} and g_{m2}, respectively. All of the transistors are operated at saturation region and R_1+R_2 is a very large value.
   (a) Please identity the feedback topology (5%)
   (b) Please derive the open-loop gain (5%)
   (c) Please derive the closed-loop gain (5%)
   (d) Please derive the open-loop input impedance (5%)
   (e) Please derive the closed-loop input impedance (5%)

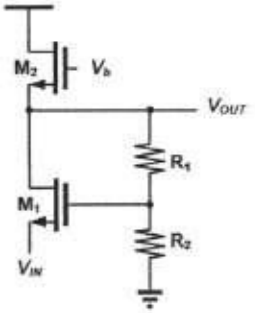

Fig. 2