

元智大學 101 學年度研究所 碩士班 招生試題卷

系(所)別： 電機工程學系碩
士班

組別： 電子工程組

科目： 電子學

用紙第 1 頁共 2 頁

● 不可使用電子計算機

1. Explain the internal power dissipation and charge sharing in VLSI circuit. (10%)

2. Explain whether a single-stage voltage amplifier can provide both maximum voltage signal and maximum power to the next stage at the same time. (10%)

3. Sketch a static CMOS logic circuit that realizes the function $Y = ABC + \overline{ABC}$. (10%)

4. For a CMOS logic-circuit family employing a 3.3-V supply.
 - (a) Suggest an ideal set of value for the threshold voltage: V_{th} , input low and high voltages: V_{IL} , V_{IH} , and output low and high voltages: V_{OL} , V_{OH} . (10%)
 - (b) Find the noise margins: NM_L , NM_H . (5%)
 - (c) Sketch the voltage-transfer characteristic (VTC). (5%)

5. As shown in Fig. 1, assume $\lambda=0$, capacitors, C_1 and C_2 , are very small, neglects all the other capacitors and transistor M_1 operates at saturation region. The transconductance of transistor M_1 is g_{m1} .
 - (a) Please Identity the feedback topology (5%)
 - (b) Please derive the open-loop gain (5%)
 - (c) Please derive the closed-loop gain (5%)
 - (d) Please derive the open-loop input impedance (5%)
 - (e) Please derive the closed-loop input impedance (5%)

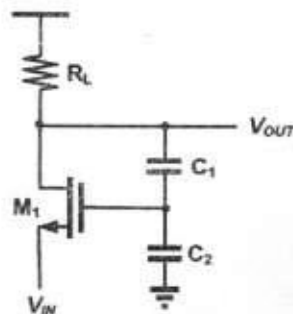


Fig. 1

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6. As shown in Fig. 2, assume $\lambda=0$ and transconductances of transistors M_1 and M_2 are g_{m1} and g_{m2} , respectively. All of the transistors are operated at saturation region.
- Please derive the gain of the circuit from node A to node B (5%)
 - At high frequency, please derive the capacitance at node A (5%)
 - Please calculate the location of pole at node A (5%)
 - Please calculate the location of pole at node B (5%)
 - Please calculate the location of pole at V_{OUT} (5%)

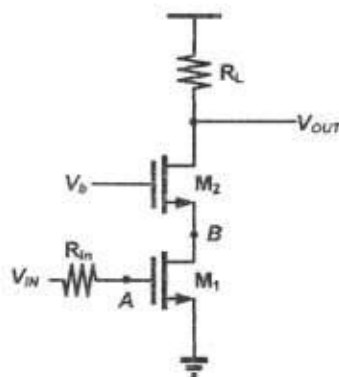


Fig. 2