(101)輔仁大學碩士班招生考試試題

考試日期:101年3月9日第3節

本試題共 1 頁 (本頁為第 1 頁)

科目:計算機系統

系所組:資訊工程研究所

Answer all the questions clearly. Each Question is worth 10 pts for a total of 100 pts.

中英文作答均可※注意: 試題須隨答案卷繳回。

- 1. a). What is thrashing? What causes it? b). How to prevent thrashing? c). Can we eliminate it from occurring?
- 2. a). What is demand paging? b). What is lazy Swapper? Explain both in detail for full grade.
- 3. Consider the reference page sequence is as follows: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5, and the number of page frame is 4? Explain and give details for the following questions below.
 - a. How many page faults would occur using FIFO algorithm?
 - b. How many page faults would occur using LRU algorithm?
 - c. How many page faults would occur using OPT algorithm?
 - d. Suppose we decrease page frame to 3, how many page faults for FIFO algorithm?
 - e. What phenomenon will occur? Explain clearly.
- 4. a). Can we implement synchronization primitives by disabling interrupts? b). Is it appropriate in a single-processor system if the synchronization primitives are to be used in user-level requirement?
- 5. Given the following three basic scheduling algorithms such as FCFS, SJF (non-preemptive), and Round Robin,
 - a. Which one is the simplest scheduling algorithm given the above? Explain
 - b. Which one is more appropriate for a time-shared system? Explain
 - c. Which one provides the shortest waiting time? Explain
 - d. Which one will cause short processes to wait for long processes? Explain
 - e. Which one is more likely to be used in OS? Why?
- 6. For the number of transistors to be quadrupled every 3 years, the line width of VLSI circuits must be reduced by how much in every 3 years?
- 7. For a MIPS assembly program consists of *beq* and *sw* instructions only, will there be any data hazards when executing the program? Please explain the reasons.
- 8. Can deeper pipelines of CPUs improve IPC(instructions per clock)? Can more pipelines per core improve IPC(instructions per clock)?
- 9. What are the advantages of a quad-channel memory controller compared to a single-channel memory controller?
- 10. When can polled I/O be used instead of interrupt-driven I/O?

- 2.本試題紙空白部份可當稿紙使用。
- 3.考生於作答時可否使用計算機、法典、字典或其他資料或工具,以簡章之規定為準。

[※] 注意:1.考生須在「彌封答案卷」上作答。