# 國立高雄大學 101 學年度研究所碩士班招生考試試題

科目：微電子學
考試時間：100 分鐘

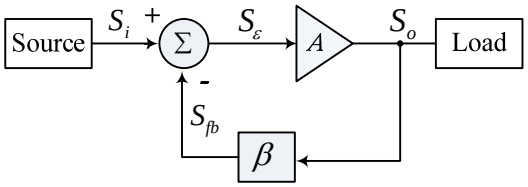
系所：
電機工程學系(微電子組)
本科原始成績：100 分

是否使用計算機：是

**注意：小訊號分析時未將電晶體小訊號模型於解答中呈現者，將不予計分。**

1. (a) Analyze and obtain the *transfer function* and *gain sensitivity* of the ideal feedback system in Fig.1(a). (4%+6%)
   (b) For ideal operational amplifier, describe the *concept of virtual ground*. (4%)
   (c). Fig.1(b) is the ideal shunt-series feedback topology, analyze and determine circuit characterizations including *closed-loop gain*, *input resistance* and *output resistance*. (10%)
   (d). Describe what is meant by *Nyquist stability criterion* for a feedback amplifier. (4%)

**Fig.1(a)**



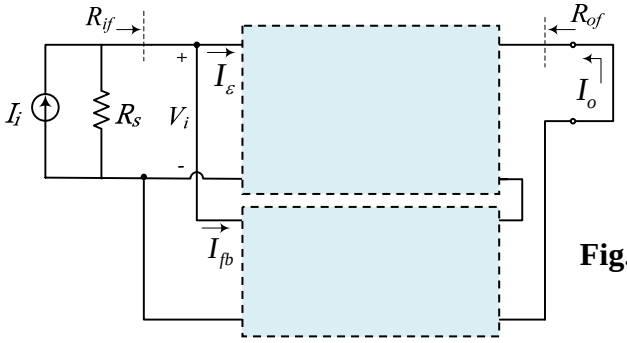
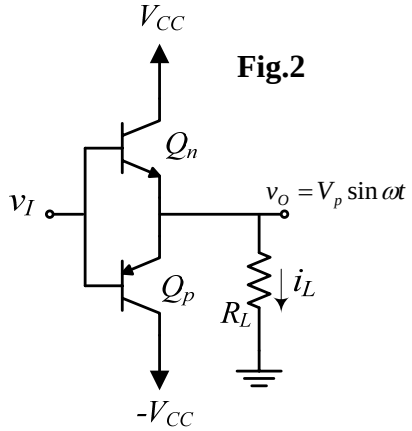




**Fig.1(b)**

2. (a) Describe what is meant by (a)*power conversion efficiency* and (b)*crossover distortion* for power amplifier. (2%+2%)
   (b). Fig.2 is a complementary push-pull output stage. If the base-emitter turn-on voltages are zero, describe and determine *the conversion efficiency*. And, when $V_p$=$V_{CC}$, the *maximum possible conversion efficiency*. (12%)

3. Fig.3 is the MOSFET cascode current mirror. Assume $I_{REF} = I_0$ and $\lambda \neq 0$. Determine the output resistance at the drain of M4. (5%)

**Fig.2**



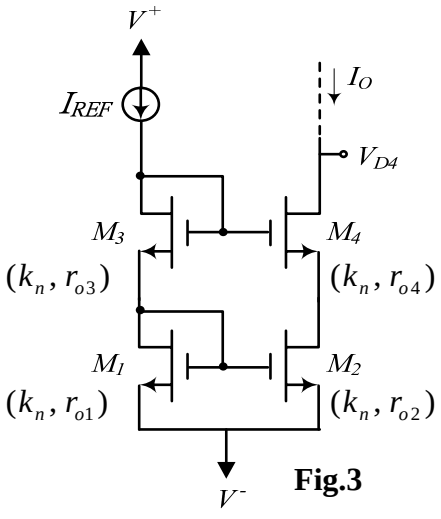




**Fig.3**

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4. Fig.4 is a basic MOSFET differential pair configuration. Assume the transistors are matched, with $\lambda = 0$ for each transistor and that the constant-current source is represented by a finite output resistance $R_0$ for small-signal analysis. ($g_{m1} = g_{m2} = g_m, k_{M1} = k_{M2} = k_n$)

(a) Determine *differential-mode gain*, *common-mode gain* and *common-mode rejection ratio*. (12%)

(b) If $V^+ = 3V, V^- = -3V, I_Q = 0.2mA, R_D = 15k\Omega, V_{TN} = 0.4V$, and $k_n' = \frac{1}{2}\mu_n C_{ox} = 100\,\mu A/V^2$. Determine the *width-to-length ratio* of the transistors such that the one-sided differential voltage gain is $A_d = 15$. (4%)

5. (a) Describe *Early voltage effect* (Base-width modulation effect) by the steady-state minority carrier concentrations for a *npn* transistor biased in the active mode. (3%)

(b) In Fig.5(a), assuming uniform doping in each region, determine the *build-in potential barrier* in terms of $N_A$ and $N_D$. (5%)

(c). In Fig.5(b), *pn* junction is biased in $V_{bias}$, assuming uniform doping in each region and $N_A > N_D$, determine *junction built-in voltage* ($V_j$) in terms of $N_A$ and $N_D$. (8%)

6. (a).Plot the *inverting operational amplifier* and *non-inverting operational amplifier*, determine *voltage gain*, *input impedance* and *output impedance* when operational amplifier is ideal. (6%+6%)

(b). Determine the *voltage gain* $\frac{v_0}{v_I}$ in Fig.6. (3%)

(c). Using the result of part (b), at what frequency is the magnitude of the gain a factor of $\sqrt{2}$ less than the high-frequency limiting value? (4%)

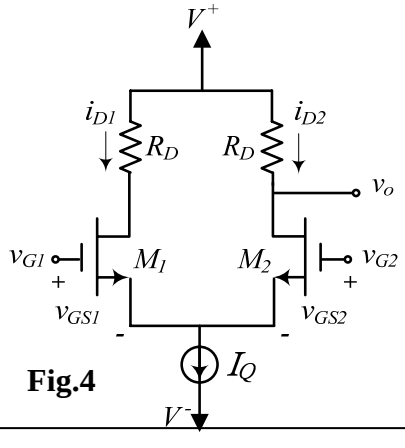


Fig.4

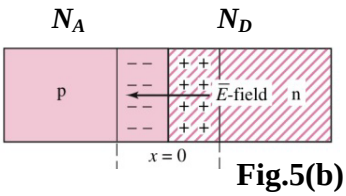


Fig.5(b)

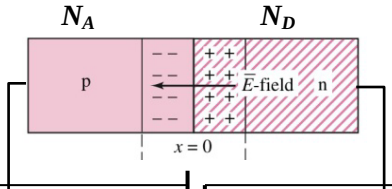


Fig.5(b)

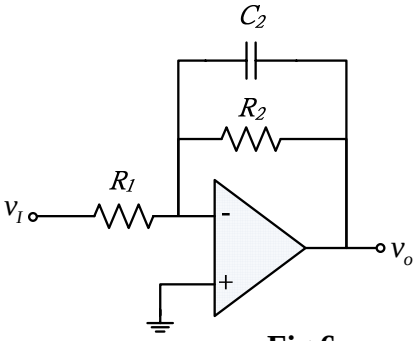


Fig.6

$V_{bias}$ 背面尚有試題

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