國　立　宜　蘭　大　學

１０１學年度研究所碩士班考試入學

電子學試題

（電子工程學系碩士班）

准考證號碼：

《作答注意事項》

1. 請先檢查准考證號碼、座位號碼及答案卷號碼是否相符。
2. 考試時間：100 分鐘。
3. 本試卷共有 6 題，共計 100 分。
4. 請將答案寫在答案卷上。
5. 考試中禁止使用大哥大或其他通信設備。
6. 考試後，請將試題卷及答案卷一併繳交。
7. 本試卷採雙面影印，請勿漏答。
8. 本考科可使用非程式型（不具備儲存程式功能）之電子計算機。

1. Choose the correct answer for the following questions. (40%)

(1) Diffusion capacitance is existed while *pn* junction is under:
(A) open circuit (B) reverse bias (C) forward bias (D) barrier.

(2) Compared with the *pn* junction under open circuit, which is correct about *pn* junction under forward bias?
(A) Diffusion current is decreased.
(B) Charge stored in depletion region is increased.
(C) Width of depletion region is increased.
(D) Barrier of depletion region is decreased.

(3) The addition of R_e in Fig.1 is used to enhance the:
(A) linear region (B) the output resistance
(C) the voltage gain (D) the transconductance.

(4) If the current gain parameter of BJT in active region is represented as β, which is correct about the current gain parameter?
(A) β is defined as I_B/I_C
(B) under the same circuit, the BJT with smaller β will saturate more easily.
(C) the value of β is not related to temperature.
(D) the current gain in saturation region is less than β.

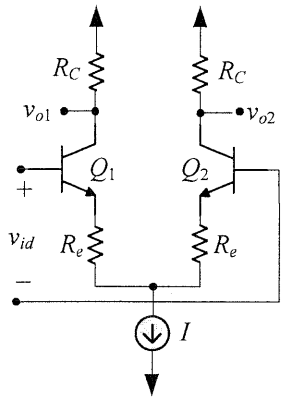


Fig.1

(5) For the Fig.2 shown is the current i_D versus v_{DS} of NMOS and the load line, which is the best bias point?
(A) point *A* (B) point *B* (C) point *C* (D) point *D*

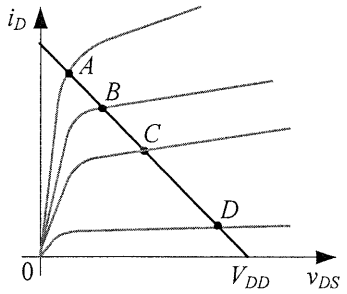


Fig.2

(6) Compared with Common-Emitter (CE) amplifier, which is correct about Common-Collector (CC) amplifier?
(A) larger voltage gain
(B) less output resistance
(C) bad frequency response
(D) often used in differential amplifier

(7) The circuit shown in Fig.3 is Widlar current source, and it is used to generate
(A) a small output current using relatively small resistors
(B) a large output current using relatively large resistors
(C) a small output current using relatively large resistors
(D) a large output current using relatively small resistors

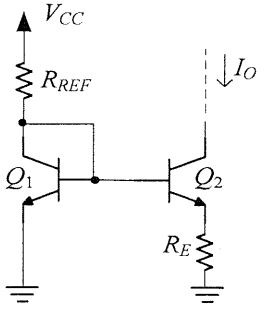


Fig.3

(8) Compared with CE, the CC-CE configuration shown in Fig.4 has main advantages on
(A) input resistance decreased and voltage gain increased
(B) voltage gain increased and output resistance decreased
(C) input resistance increased and bandwidth increased
(D) output resistance increased and bandwidth increased

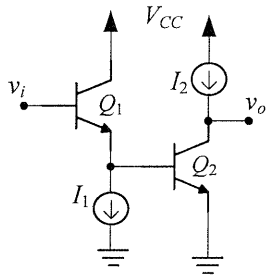


Fig.4

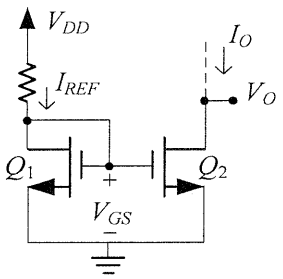


Fig.5

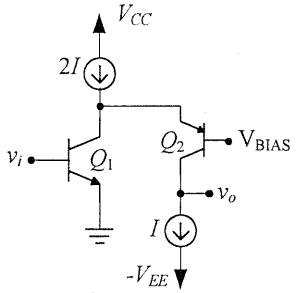


Fig.6

(9) For the current mirror shown in Fig.5 and I_{REF} = 40 μA, assume Q_1 and Q_2 are identical with V_t = 0.5 V, $\mu_n C_{ox}(W/L)$ = 20 μA/V^2. If this circuit can work properly, which is the minimum value of voltage V_O in V? (A) 2.5 (B) 2.0 (C) 1.5 (D) 0.5

(10) For the folder cascode amplifier shown in Fig.6, assume the current gain parameters and the transconductances of Q_1, Q_2 are β_1, β_2 and g_{m1}, g_{m2}, respectively. Then the voltage gain $A_v = v_o/v_i$ =?
(A) $-g_{m2}\beta_1 r_{o1}$ (B) $-g_{m2}\beta_2 r_{o2}$ (C) $-g_{m1}\beta_1 r_{o1}$ (D) $-g_{m1}\beta_2 r_{o2}$

2. The BJT circuit shown in Fig.7 has the following condition: V_{CC} = +15 V, β = 100, R_{B1} = 100 kΩ, R_{B2} = 50 kΩ, R_C = 5 kΩ, R_E = 2 kΩ. Find:
(a) current I_C , and
(b) its transconductance g_m.
(10%)

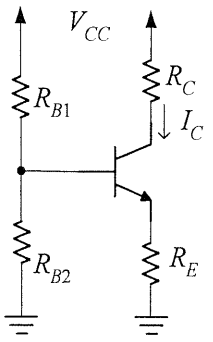


Fig.7

3. For the circuit shown in Fig.8, find:
(a) transfer function $V_o(s)/V_i(s)$.
(b) Design the circuit to obtain a dc gain = 20 dB, 3-dB frequency ω_0 = 10k rad/s, and R_i = 1 kΩ.
(10%)

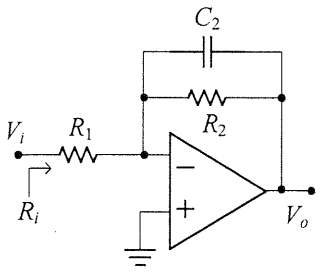


Fig.8

4. For the circuit shown in Fig.9, assume the diodes to be ideal. Analyze and plot the voltage transfer characteristic of the circuit.
(10%)

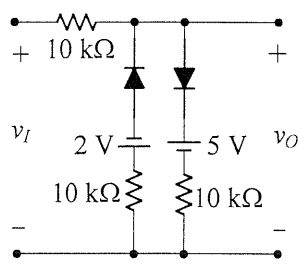
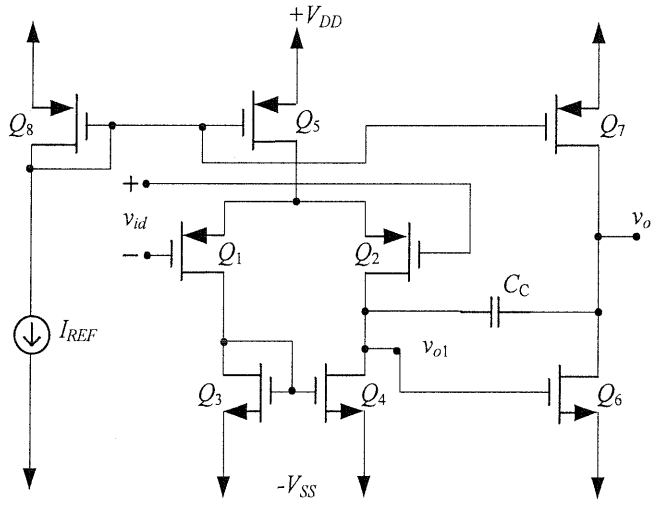


Fig.9

5. The circuit shown in Fig.10 has the following parameters: I_{REF} = 200 μA, $|V_t|$ = 1 V, V_{DD} = V_{SS} = 5 V, $\mu_n C_{ox}$ = 160 μA/V^2, $\mu_p C_{ox}$ = 40 μA/V^2, $|V_A|$ = 20 V. Find:
(a) the $|V_{GS}|$ of Q_1, Q_3, Q_5
(b) the input common-mode range
(c) the transconductance g_m of Q_2
(d) voltage gain v_{o1}/v_{id}.
(20%)



Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	20/1	20/1	5/1	5/1	40/1	10/1	40/1	40/1

Fig.10

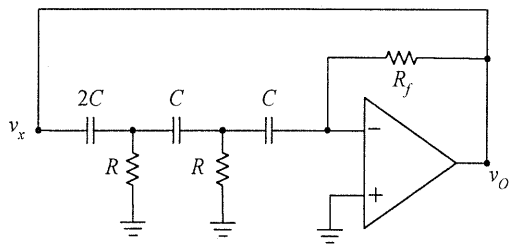


Fig.11

6. For the oscillator circuit shown in Fig.11, (a) find the loop gain $A\beta = V_o(j\omega)/V_x(j\omega)$.
(b) Find the frequency of oscillation ω_o and the minimum required value of R_f for oscillation to start.
(10%)