國立臺北科技大學 103 學年度碩士班招生考試

系所組別：2300 資訊工程系碩士班

第二節　計算機概論　試題

> **注意事項：**
> 1. 本試題共五題，配分共 100 分。
> 2. 請標明大題、子題編號作答，不必抄題。
> 3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一、(15%) Multiple Choice

1.　(3%) What is the purpose of a compiler?
　　A.　translate machine language into assembly language
　　B.　translate FORTRAN into COBOL
　　C.　translate machine language into FORTRAN
　　D.　translate application programs into system programs
　　E.　translate high-level language into machine language

2.　(3%) You can use at least how many NAND Gates to build a AND gate?
　　A.　1
　　B.　2
　　C.　3
　　D.　4
　　E.　5

3.　(3%) Which gate produces a 1 ONLY if both inputs are 0
　　A.　AND
　　B.　NAND
　　C.　XOR
　　D.　OR
　　E.　NOR

4. (3%) Match the solution with the problem

   1111011 + 111001 (binary addition)

   1111111 + 11111 (binary addition)

   1100111 − 11111 (binary subtraction)

   (1) 10110100 (2) 10011110 (3) 11011010

   (4) 1001000   (5) 1011000   (6) 10000000
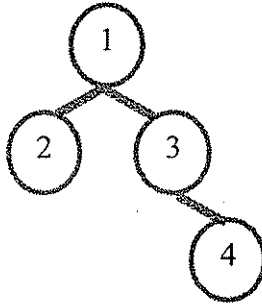
   A. (1)(6)(4)
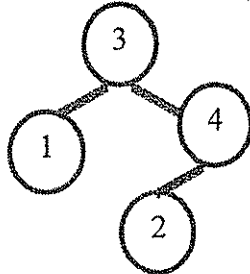
   B. (1)(2)(4)

   C. (1)(2)(5)

   D. (6)(2)(4)

   E. (3)(1)(5)

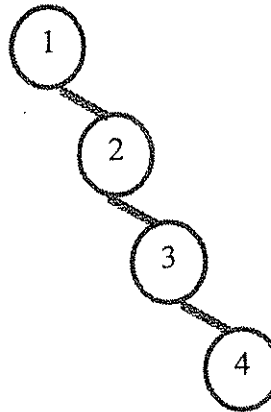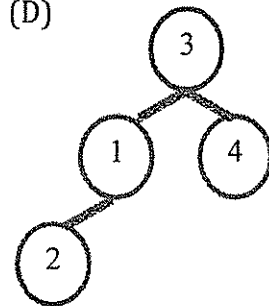5. (3%) Which of the following trees is a binary search tree?

二、(25%) Short answer

1. (5%) How is the decimal number 0.76 represented in binary? (to the 9th decimal place)

2. (5%) The table below listed 4 jobs and their arrival times and how many CPU times they need to finish.

Job	Arrival time	CPU time
1	0	8
2	2	3
3	3	12
4	4	5

   If the CPU scheduling is shortest-remaining time-first algorithm, then how long is the average waiting time?

3. (5%) use the following array of values.

	[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]
list	23	41	66	20	2	90	9	34	19	40	99

Show the state of the list when the first recursive call is made in Quicksort using list[0] as split value.

Array when first recursive call is made.

	[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]

4. (5%) use the following array of values.

	[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]
list	5	7	20	33	44	46	48	49	101	102	105

How many comparisons does it take using a binary search to find the value 44 or determine that the item is not in the list?

5. (5%) What are the prefix representation and the postfix representation of the following: A*B+C /(D-E)

三、(15%) Mark the following statements as True (O) or False (X). **Explain the reasons and make corrections if the statements are false.**

1. (3%) An optical fiber can provide much wider bandwidth than that by a twisted pair copper wire. Therefore, for the same link distance, the propagation delay time incurred by using the optical fiber is much shorter than that incurred by using the twisted pair copper wire.

2. (3%) The UDP (User Datagram Protocol) transport layer protocol is often employed to support real-time multimedia applications, because it can provide the reliable connection between two communication entities.

3. (3%) In the datagram packet switching network, packets belonging to the same session will follow the same route to reach their destination nodes such that in-sequence services can be achieved.

4. (3%) The ARP (Address Resolution Protocol) is used for the user-specified hostname (such as www.ntut.edu.tw) and IP address mapping. Therefore, the ARP message is usually carried in the IP packet for transmission.

5. (3%) The MAC (Multiple Access Control) mechanism is mainly used to provide error and flow control capabilities for transmission in the LAN (Local Area Network) environment.

四、(15%) Please answer the following problems about the multitasking issues of an operating system running on a single-core processor machine.

1. (5%) When you desire to implement an operating system, the processes are essential execution elements in your system. Can you list and express all the states that a typical process may be in, and illustrate and explain a state transition diagram of a process?

2. (5%) In an operating system, the processes are the fundamental execution instances of the programs. What is the necessary way to execute multiple processes by sharing the CPU time of a single-core processor system? What are the necessary context information that a process should store so that its execution can be resumed from the same point at a later time?

3. (5%) When we execute multiple processes of programs on a single-core processor system, we may find that the switches between the processes may take significant computing times. To save the computational costs, we may re-write the program to execute multiple threads in a process. Therefore, what are the differences between the context of a process and that of a thread, and what are the advantages of using threads on a single-core processor system?

五、(30%) Given the following MIPS assembly code segments in Figure 1, which contain a double loop. Please answer the following problems.

MIPS Code	addi $s0, $zero, 0
	beq $zero, $zero, OUT_LOOP_TEST
	OUT_LOOP :
	addi $s1, $zero, 0
	beq $zero, $zero, IN_LOOP_TEST
	IN_LOOP :
	sll$t2,$s0,2
	add$t2, $t2,$s2
	lw$t3,0($t2)
	sll$t4,$s1,2
	add$t4,$t4,$s3
	lw$t5,0($t4)
	add$t5,$t5,$t3
	sw$t5, 0($t4)
	addi$s1,$s1,1
	IN_LOOP_TEST :
	slti $t0, $s1, 10
	bne$t0,$zero, IN_LOOP
	addi$s0,$s0,1
	OUT_LOOP_TEST :
	slti $t0, $s0, 5
	bne$t0,$zero, OUT_LOOP

Figure 1. MIPS assembly code segment

1.　(6%) What is the **equivalent C code** of the above MIPS assembly code in Figure 1? Please disassemble the MIPS code into the **equivalent C code**. Assume that the C-level integer i, j are held in the registers $s0 and $s1, respectively, and the base addresses of the integer arrays A, B are held in the registers $s2, and $s3, respectively.

2. (10%) Then, given a typical MIPS processor with a five-stage pipeline, including: (1).IF-Instruction fetch; (2).ID-Instruction decode and register fetch; (3).EX-Execution or calculate effective address; (4).MEM-Access data memory; and (5).WB-Write back to registers. Assume that the register-write is done in the first-half of a clock cycle, and the register-read can be done in the second-half of the cycle, and all branch outcomes are determined in the ID stage, but there is **no forwarding, no hazard detection, no branch-predictor, and no delayed slots**. Now we want to execute the **MIPS code** in Figure 1 using this pipeline. How many **clock cycles** will the program take to complete the codes due to possible hazards?

3. (4%) Next, to improve the execution performance of the abovementioned five-stage pipelined processor due to data and control hazards, we now add the full hazard detection and forwarding units for possible data and control hazards, as well as a **dynamic branch-predictor**. Can you indicate that the **branch prediction** should be conducted in which pipeline stage to reduce possible stalls?

4. (10%) Now, to further speed-up the execution performance, suppose that we now have an above-mentioned five-stage pipeline with **full data hazard detection and forwarding units** (i.e. forward all results that can be forwarded), and the branches are decided in the **ID stage** with a **two-bit branch predictor** as depicted in Figure 2, and **no delay slots**. Now, how many **clock cycles** will the program in Figure 1 need to execute the MIPS codes using this pipeline? Assume that the **predictor** starts off in the **top-left state** in Figure 2 (predict taken).
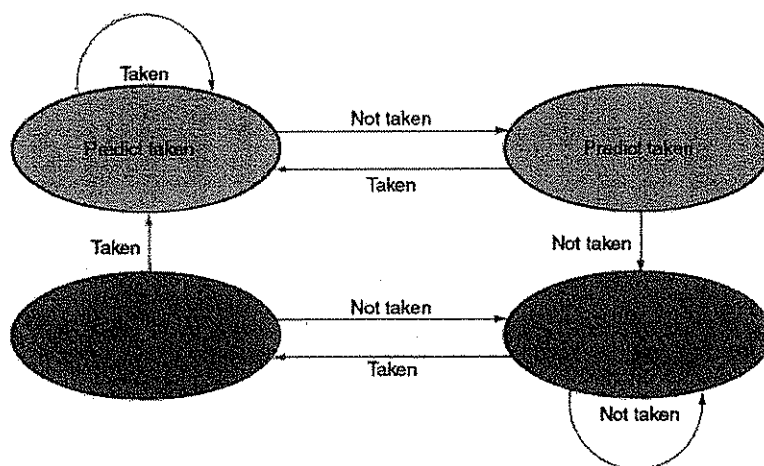

Figure 2. The two-bit branch predictor