國立臺灣師範大學 **103** 學年度**碩士班**招生考試試題

科目：計算機系統　　　　　　　　　適用系所：資訊工程學系

注意：1.本試題共 **3** 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則不予計分。

1. Consider the following code sequence.

SUB	R1, R4, R3;	R1 ← R4-R3
ADD	R5, R1, R6;	R5 ← R1+R6
LW	R8,12(R6);	R8 ← MEM[12+R6]
ADD	R9, R5, R8;	R9 ← R5+R8
SW	R9,16(R6);	MEM[16+R6] ← R9

Suppose the code sequence is executed in a five-stage (IF, ID, EX, MEM and WB) MIPS pipeline processor **with hazard detection and data forwarding units.** Assume the processor includes separate instruction and data memories so that the structural hazard for memory references can be avoided.

(a) (5 分) Identify all the data hazards which can be solved by forwarding.

(b) (5 分) Identify all the data hazards which can **not** be solved by forwarding.

(c) (5 分) Determine the total number of clock cycles required for the execution of the code sequence.

(d) (5 分) Suppose the clock rate of the MIPS processor is 1GHz. Find the CPU time of the code sequence (in terms of ns).

2. Consider the following code sequence.

ADD	R1, R2, R3;	R1 ← R2+R3
ADD	R3, R4, R5;	R3 ← R4+R5
LW	R6,32(R8);	R6 ← MEM[32+R8]
LW	R7,36(R8);	R7 ← MEM[36+R8]
ADD	R9,R6,R1;	R9 ← R6+R1
ADD	R10,R7,R3	R10 ← R7+R3
ADD	R11,R9,R10	R11 ← R9+R10
LW	R12,40(R8)	R12 ← MEM[40+R8]

Suppose the code sequence is executed in a five-stage (IF, ID, EX, MEM and WB) MIPS pipeline processor **with separate instruction and data memories.**

(a) (5 分) Determine the number of accesses to the instruction memory.

(b) (5 分) Determine the number of accesses to the data memory.

(c) (5 分) Suppose the execution of the code sequence produces 3 misses: 2 misses in the instruction memory, and 1 miss in the data memory. Determine the miss rate of the instruction memory. Determine the miss rate of the data memory.

(d) (5 分) Suppose the hit time of the instruction and data memories is 1 clock cycle.

The miss penalty is 100 clock cycles. Based on the results in part (c), please compute the average memory access time (in terms of clock cycles) of instruction and data memories, respectively.

3. Briefly explain the following terms.
(a) (2 分) Control hazard,
(b) (2 分) Direct mapped cache,
(c) (2 分) Fully associative cache,
(d) (2 分) Translation lookaside buffer (TLB),
(e) (2 分) Direct memory access (DMA).

4. **Processes** in the system move in different states, e.g., "new" and "terminated". Please answer the following questions.
(a) (5 分) Illustrate the diagram of process state and explain each state transition in detail.
(b) (9 分) Please list at least three other process states and show their relationship. At the same time, please define "short-term scheduling," "mid-term scheduling," and "long-term scheduling."

5. Please answer following questions about **CPU scheduling**:
(a) (4 分) Please define "FIFO/FCFS" and "Round Robin" scheduling algorithms.
(b) (10 分) Please draw the *Gantt Chart* and compute the *average waiting time* of the execution of the following processes with the Round Robin scheduling with time slice = 3 time units.

Process	CPU execution time	Arrival time
P1	5	2
P2	6	0
P3	3	4
P4	4	5

6. Please answer following question about **synchronization**:
   (a) (3 分) What is a critical-section?
   (b) (3 分) What are the three requirements of critical-section?
   (c) (3 分) What is busy waiting?
   (d) (4 分) What is the advantage and disadvantage of busy waiting?

7. Given a computer system with a 32-bit virtual address, 4KB pages, and 8B per page entry of a page table. Suppose that the number of bits of physical addresses is 48, and the system is byte-addressable. If multiple-level paging is implemented, please answer the following questions:
   (a) (4 分) What is the maximum number of (physical) page frames in the system, where each page frame is the container to store the data of one (virtual) page? What is the maximum number of pages for a process?
   (b) (5 分) Suppose that the multi-level paging is adopted. How many levels do we need?