國立中正大學 101 學年度碩士班招生考試試題

電磁晶片組

系所別：電機工程學系- 計算機工程組　　科目：電子學

晶片系統組

第 2 節　　

1. Please draw the cross section of the PMOS transistor operating in the saturation region. Please mark the depletion region and the induced channel. What is the major charge carrier in the induced channel? (10%)

2. Design a non-inverting amplifier, shown in Fig. P2, for the following specifications: closed-loop gain = 4, gain error = 1%, closed-loop bandwidth = 100MHz.

   (a) Determine the required R_1, R_2, and open-loop gain and bandwidth of the op amp.(8%)

   (b) Explain what happens if op amp exhibits an offset of 20mV. (2%)

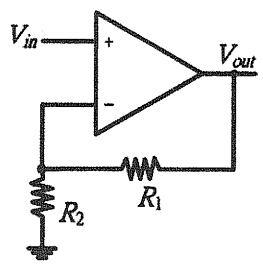

Fig. P2

3. Calculate the voltage gain of the circuit shown in Fig. P3. M_1 is identical with M_2, and given V_{DD}=3V, V_b=2V, V_t=0.6V, $\mu_n C_{OX}(W/L)$=240 μA/V², I_1 = 3 mA, R_D = 0.5 kΩ, and λ = 0. (10%)

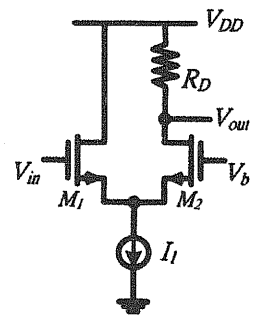

Fig. P3

4. A CMOS op amp, shown in Fig. P4, is found to have a slew rate of 60 V/μs and a unity-gain bandwidth f_t of 100 MHz.

   (a) Estimate the value of the overdrive voltage of Q_1 and Q_2. (5%)

   (b) Given I_{D5} = 100 μA, calculate the value of C_C. (5%)

   (c) A resistance R = 300Ω is put in series with C_C to place the zero at infinite frequency. Calculate the required G_{m2}, which is the equivalent transconductance of the 2nd stage. (5%)

   (d) What is the maximum allowed capacitance at v_o to have a 75° phase margin? (5%)

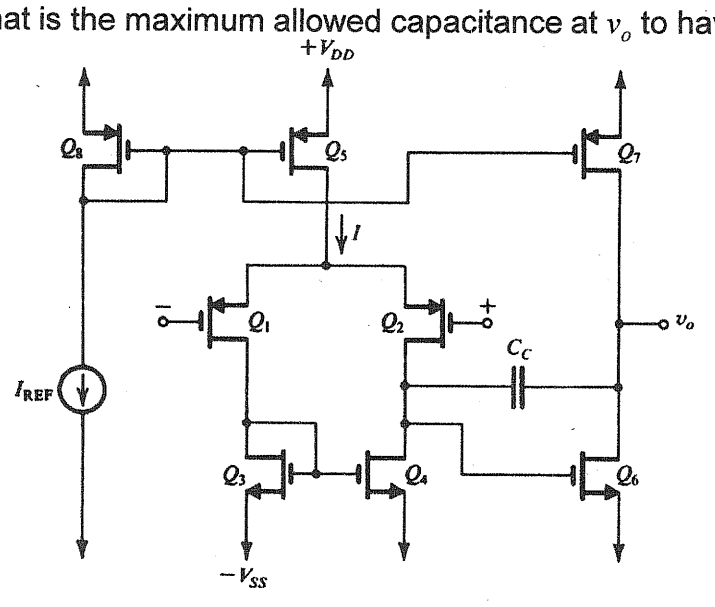

Fig. P4

5. Design of A Digital Logic Inverter (20%)

A digital logic inverter is shown in Fig. P5(a), and the transistor Q is fabricated with the following process parameters: $C_{ox}\mu_n$ = 100 μA/V², λ = 0, and V_{tn} = 0.5V.

(a) Please determine the W/L value of Q and resistance R_D to provide a 0.1V output low level (V_{OL}) and a static current of 100μA. (4%)

(b) As the circuit designated in (a), find the low-to-high propagation time (t_{PLH}) if the load capacitance *C* in Fig. P5(a) is 100fF and v_I has a zero fall time as shown in Fig. P5(b). (4%)

(c) Please sketch the voltage transfer curve (VTC) of the circuit in Fig. P5(a) and use the VTC to explain the concept of noise margin. (4%)

(d) Use the known parameters to derive the expressions of the output high level (V_{OH}), and the maximum value of input interpreted by the inverter as a logic 0 (V_{IL}). (4%)

(e) How to improve the noise margin of the logic inverter shown in Fig. P5(a). (4%)

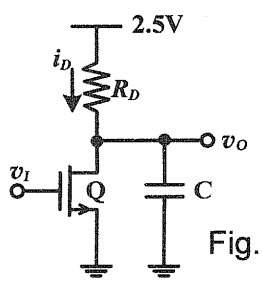

Fig. P5(a)

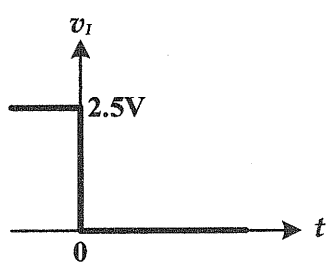

Fig. P5(b)

6. Assume that the circuit in Fig. P6 is designated to have a 200kΩ output resistance (R_{out}) and a bias current of 0.5mA with the following process parameters: $C_{ox}\mu_n$ = 100 μA/V², λ = 0.1V⁻¹, and V_{tn} = 0.4V.

(a) If Q_1 and Q_2 are identical, find their W/L. (6%)

(b) Find the required value of V_{b1}. (5%)

(c) Complete a wide-swing current mirror circuit of Fig. P6 by exposing the possible circuitry in the Black Box and explain how the "wide-swing" is achieved. Note: wide-swing means that V_o is permitted to swing as low as two overdrive voltage (2 V_{OV}). (7%)

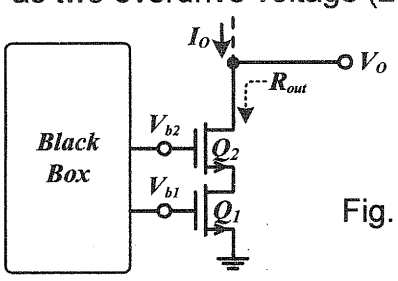

Fig. P6

7. (a) For the differential amplifier shown in Fig. P7, please derive the low-frequency common mode gain (A_{cm}). (7%)

(b) If R_{SS} = 100KΩ and C_{SS} = 0.2pF. Find the 3-dB frequency of the CMRR. (5%)

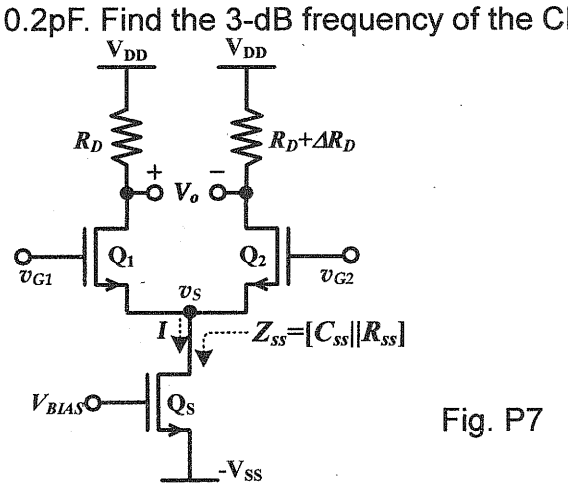

Fig. P7