國立交通大學 97 學年度碩士班考試入學試題

科目：電子學(1801) 电机与控制工程学、乙组、丙组、　　考試日期：97 年 3 月 8 日 第 2 節

系所班別：電控系跨組聯招　　組別：電控聯招　　

【可使用計算機】＊作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

1. (20% in total) Consider the MOSFET class-AB output stage shown in Fig.1. The parameters are $V_{BB}=3\ V$, $V_{DD}=10\ V$ and $R_L=20\ \Omega$. The transistors are matched, and the parameters are $k'_n(W/L)_n= k'_p(W/L)_p=0.4\ A/V^2$ and $|V_t|=1\ V$.

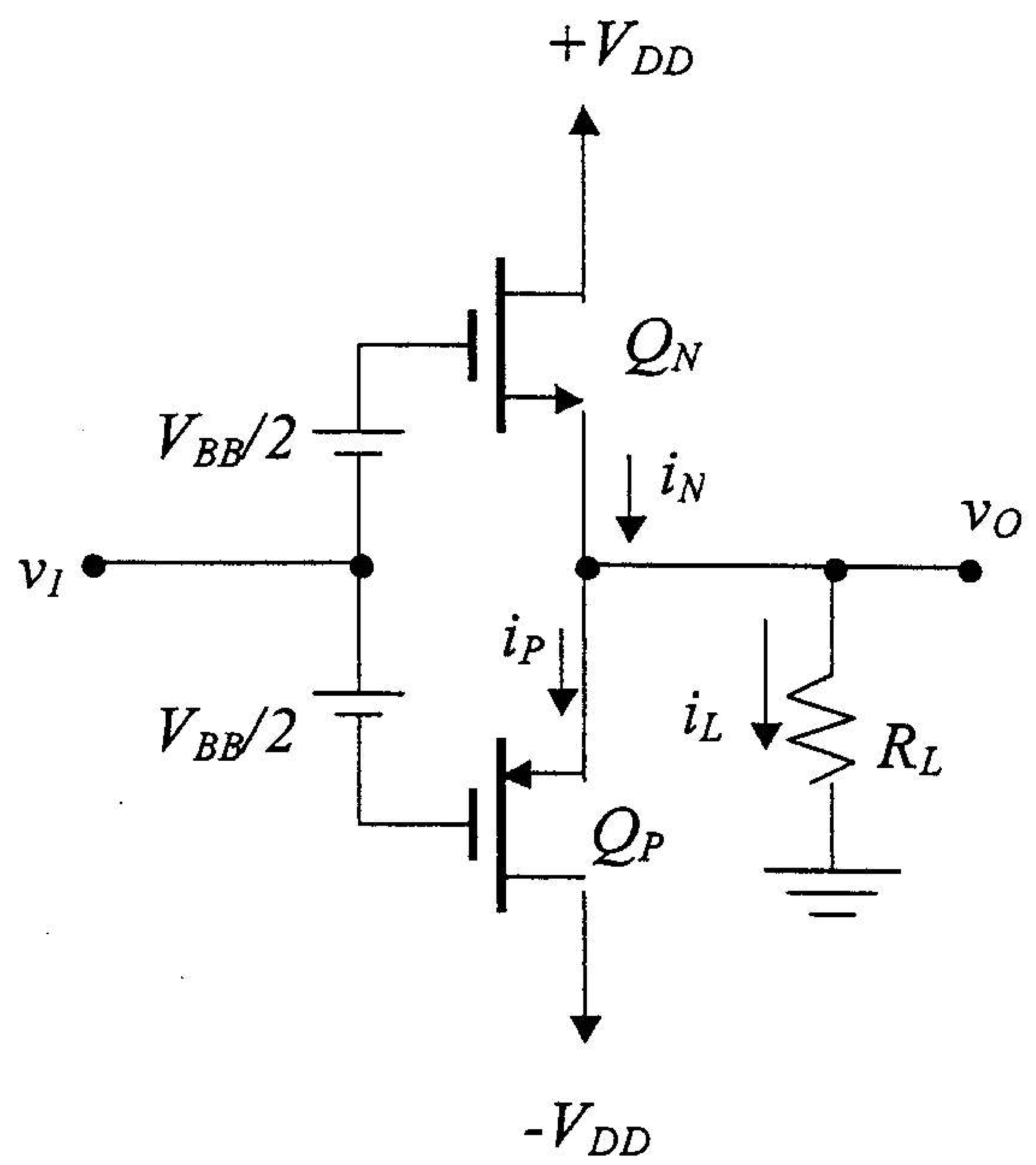


Fig.1

Let $V_{BB}=3$ V.

(a) (4%) Determine the quiescent drain current (when $v_O=0$).

(b) (8%) Determine the small-signal voltage gain A_v evaluated at $v_O=0$.

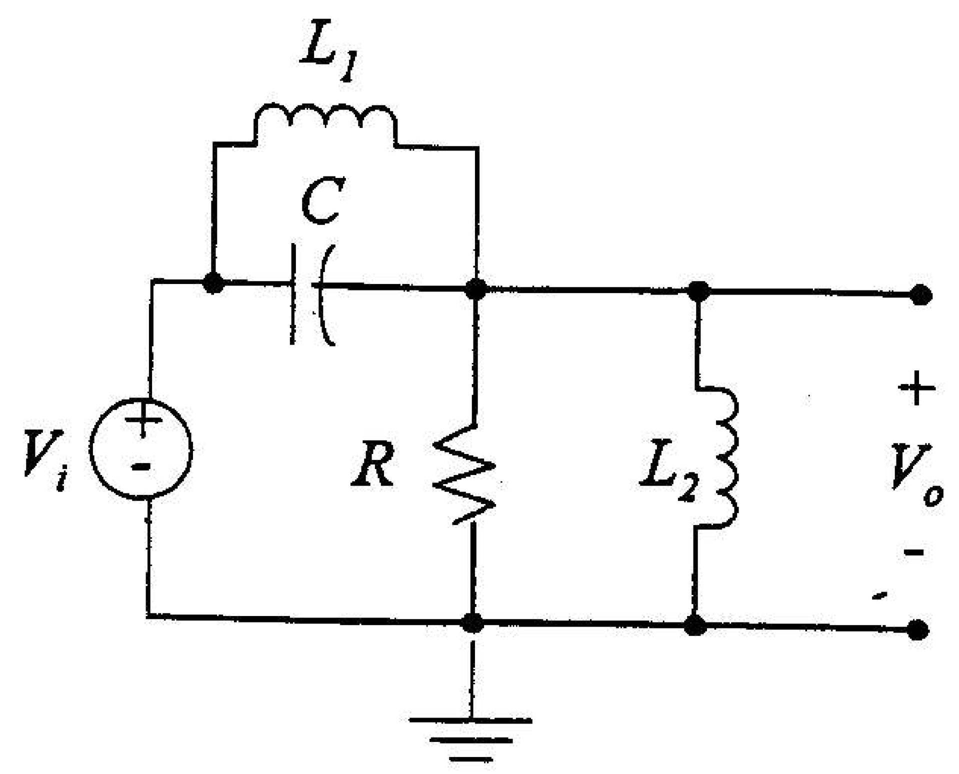
(c) (8%) Determine the small-signal voltage gain A_v evaluated at $v_O=5V$.

2. (15% in total) Consider the following circuits shown in Fig. 2.

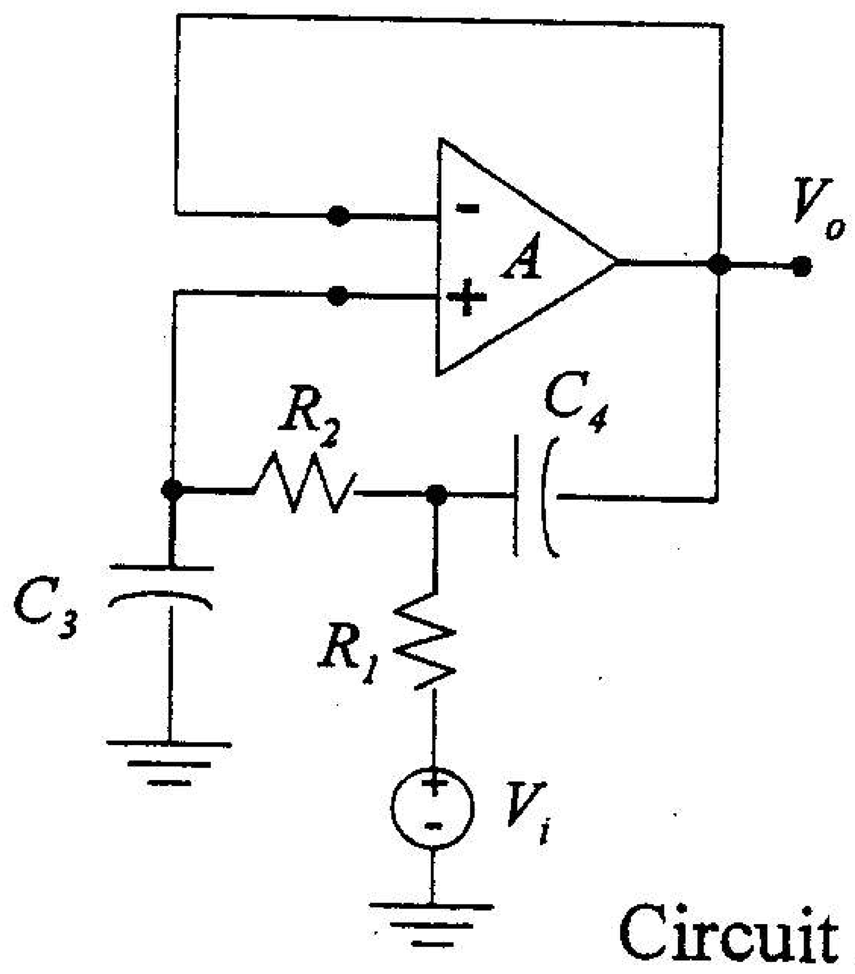
(a) (6%) The circuit A is a HPN filter. Please determine the notch frequency ω_n and the pole frequency ω_0 in terms of L_1, L_2, C, or R.

(b) (3%) What is the filter type of the circuit B?

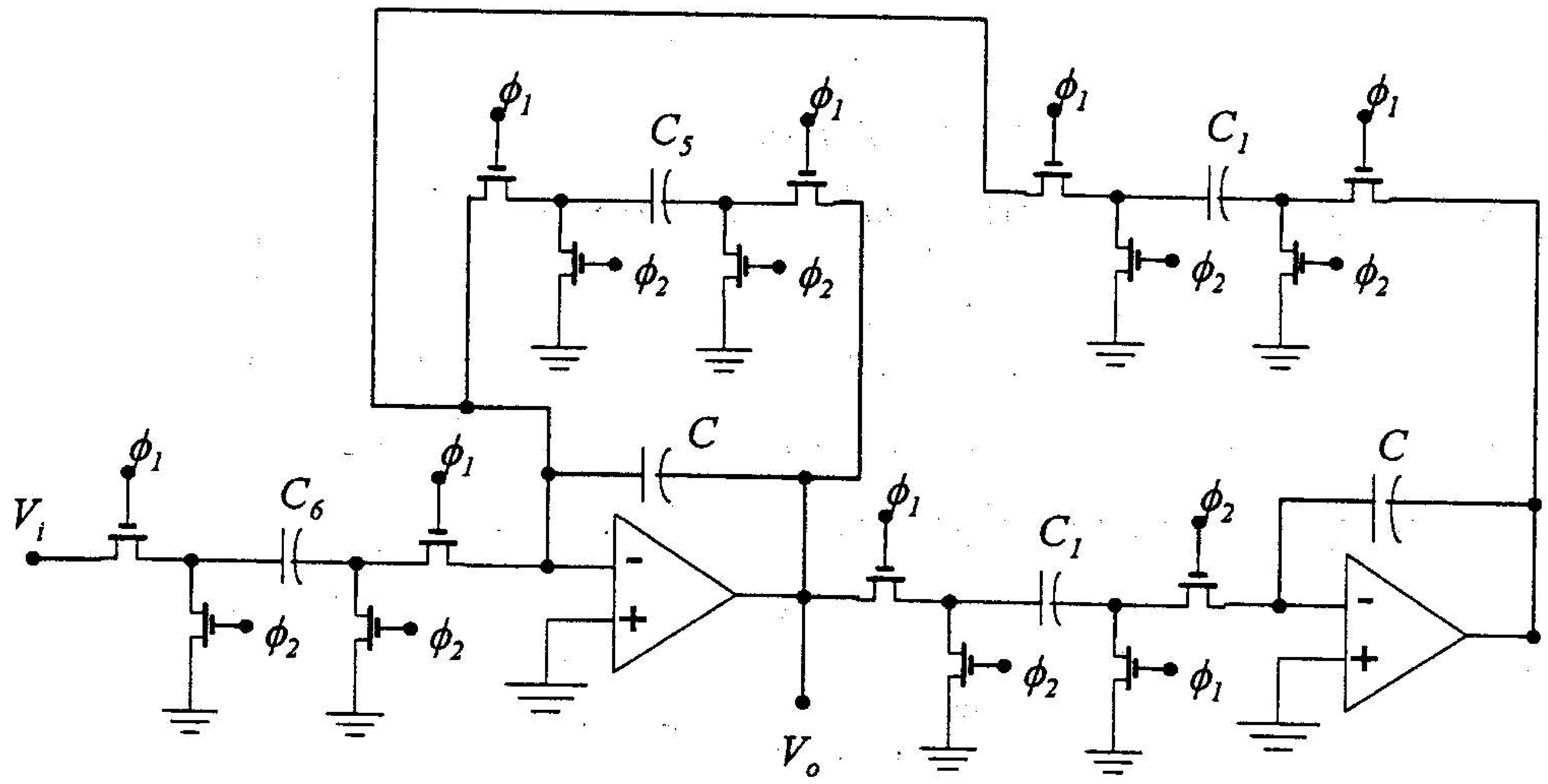
(c) (6%) Let ϕ_1 and ϕ_2 be two non-overlapped clock signals. What is the filter type of the circuit C? Given the equivalent resistance R_{eq} of a switched-capacitor circuit is equal to T_c/C_{sw} where T_c is the clock period and C_{sw} is the switched-capacitor, please determine ω_0 in terms of C, C_1, and T_c.



Circuit A



Circuit B



Circuit C

Fig. 2

3. (17% in total)

(a) Design an op-amp with feedback network in Fig. 3 (a).

i. If the open-loop gain (A) is equal to 10^4 and the close-loop gain (A_f) is equal to 10, find the value of R_2/R_1. (2%)

ii. If $V_S=1V$, find $V_o=?$ $V_f=?$ and $V_i=?$(6%)

iii. How large is the value of $\Delta A_f/A_f$ when the value of A is decreased 20%? (2%)

(b) Find the equivalent output resistance in Fig. 3(b). V_{in} is the input signal and V_o is the output signal. (7%) (Hint: Express it by g_{m1}, g_{m2}, r_{o1}, and r_{o2})

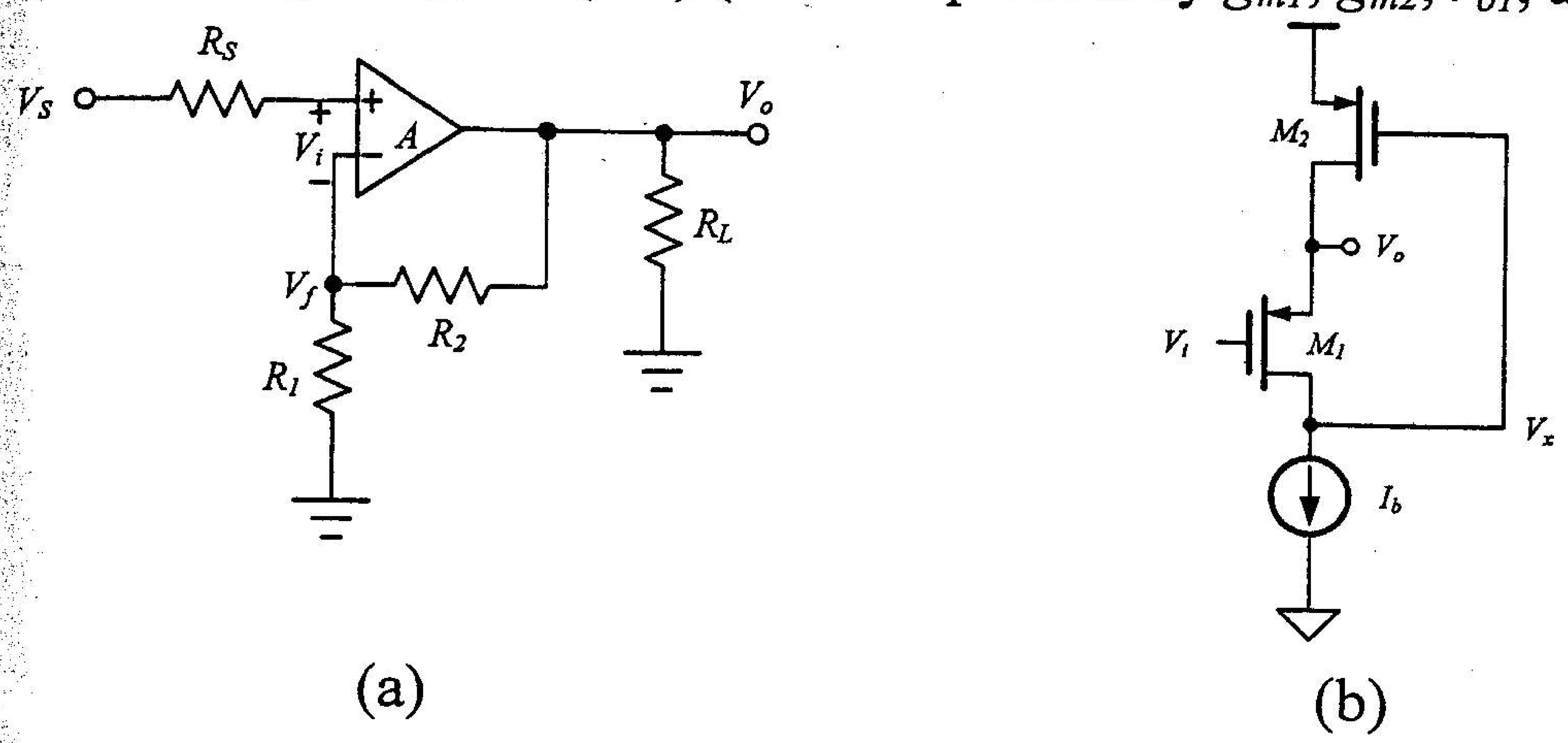


Fig. 3.

4. (16% in total) The threshold voltages of transistors M_1~M_8 are V_{TH1}~V_{TH8} in Fig.4. V_{in} is the input signal and V_b is a biasing voltage for biasing the gates of transistors M_3 and M_4.

i. Describe the function of the circuit in Fig. 4. (4%)

ii. Find out the V_{out} range that the circuit can correctly operate when V_{in} is increased from 0V to V_{DD}. (12%) (Hint: V_{DD} is high enough to provide suitable voltage headroom. Express the range by V_{GS}, V_{TH})

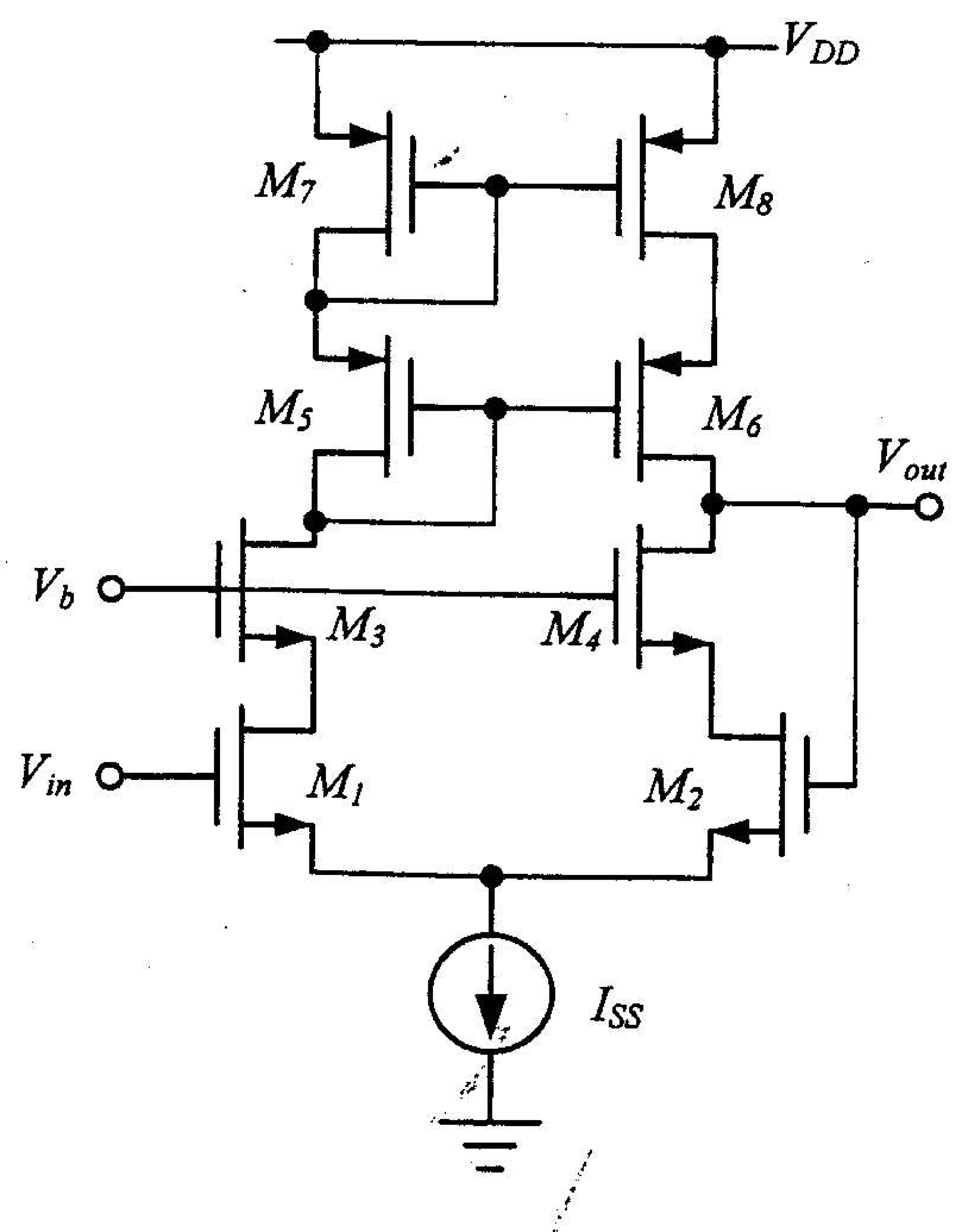


Fig. 4.

5. (18% in total) **D1** and **D2** shown in Fig. 5 are identical. They have zero on-resistances and a constant voltage drop of 0.7V when being forward biased. Ignore their reverse biased currents. The threshold voltages of **M1** and **M2** are V_{th1}= -0.6V and V_{th2}=0.6V, respectively, and $\mu_p C_{ox}(W/L)_{M1}=\mu_n C_{ox}(W/L)_{M2}=1mA/V^2$.
Let V1(t=0) and Vo(t=0) be 0V, C1=C2=1μF, V_{DC}=1.2V, and ϕ be the waveform shown in Fig. 5.
(a) Find V1 at t=0.99 sec (4%)
(b) Find Vo at t=1.99 sec (5%)
(c) Find V1 at t=3.99 sec (4%)
(d) Find Vo at t=3.99 sec (5%)

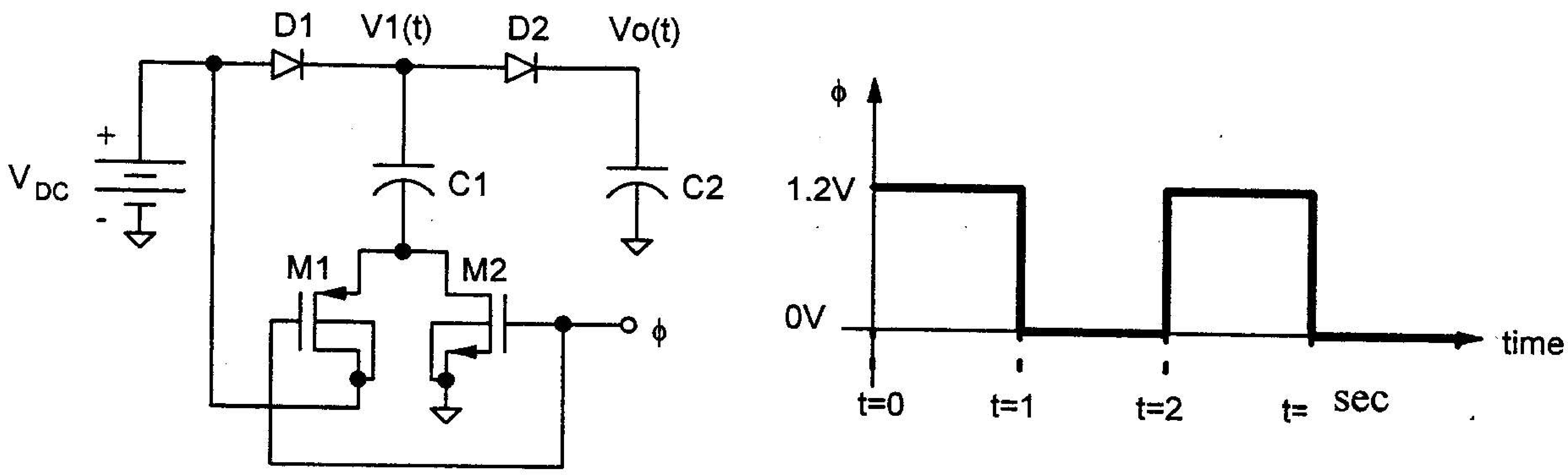


Fig.5

6. (14% in total) Refer to Fig.6, let **M1** and **M2** be identical whose threshold voltages are 0.5V and $\mu_n C_{ox}(W/L)_{M1}=\mu_n C_{ox}(W/L)_{M2}=200\ \mu A/V^2$. Meanwhile, **M3** and **M4** have the same threshold voltage of *-0.5V* and $\mu_p C_{ox}(W/L)_{M3}=200\mu A/V^2$, $\mu_p C_{ox}(W/L)_{M4}=50\mu A/V^2$. Given ***RS*** = 20KΩ and V_{DC}=3.3V. This circuit has two static states.
(a) Find I_{DS1} in both static states. (7%)
(b) Find V_{G3} and V_{G1} in both static states. (7%)

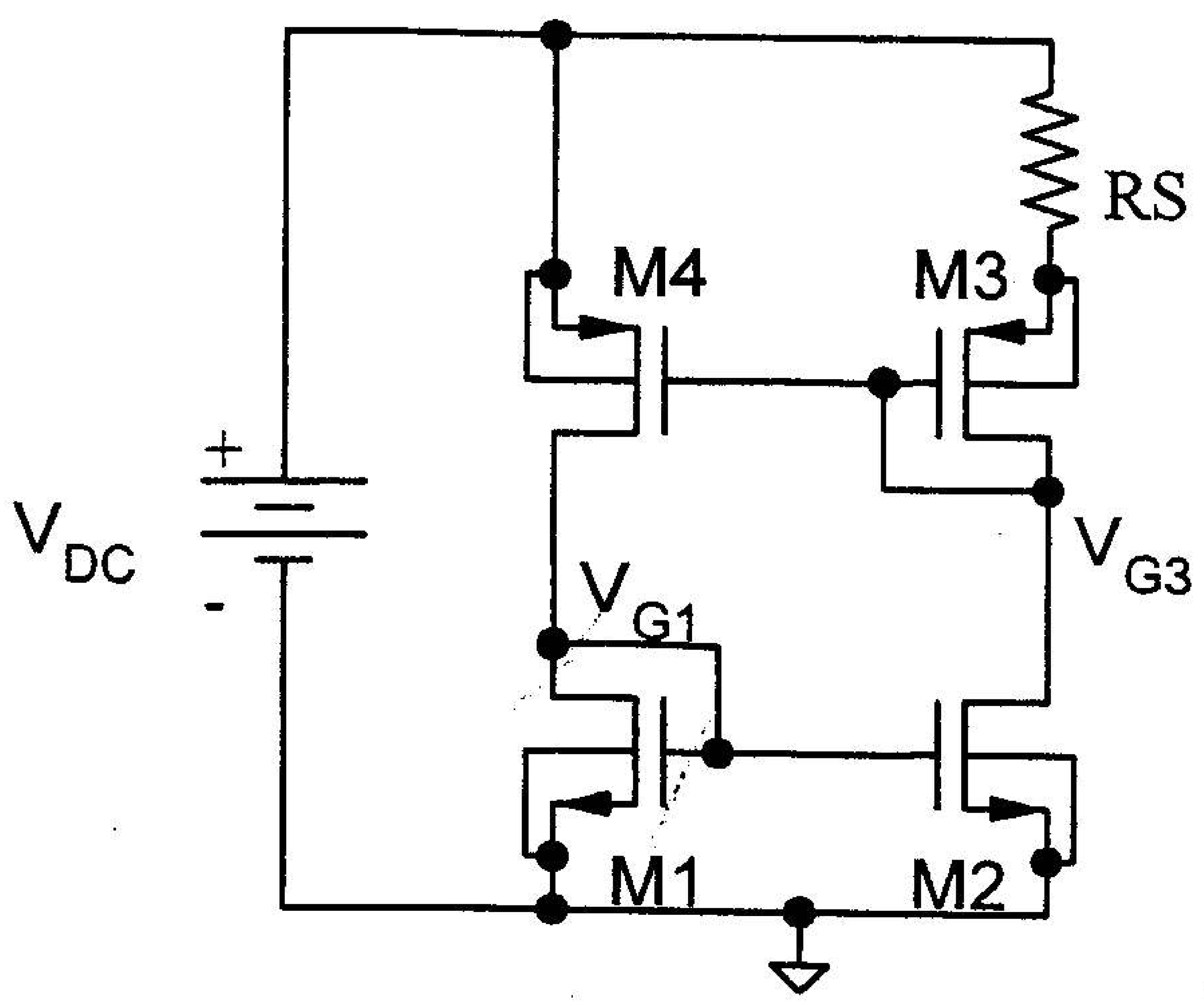


Fig. 6