國立中山大學 101 學年度碩士暨碩士專班招生考試試題

科目：數位電路【電機系碩士班丙組選考、庚組】

[Problem 1] Short answer questions:
(a) What are the differences between a combinational circuit and a sequential circuit? (4%)
(b) What are the differences between a latch and a flip-flop? (2%)
(c) What are the setup time and the hold time of a D flip-flop? (4%)
(d) What is a clocked synchronous sequential circuit? (3%)
(e) What are the differences between Mealy and Moore finite state machines? (2%)

[Problem 2] Draw the logic diagram of the following Boolean function using a multiplexer:
(a) $F(A, B, C, D) = A'B'C'+A'B'D'+A'C'D+ABCD'+AB'C'D'+AB'CD$. (5%)
(b) $F(A, B, C, D) =(A+B+D')\,(A+C'+D')\,(A'+B+C')$. (5%)
Please note that the input code words (A, B, C, D) and their complements can be used directly as fan-in in the logic circuit, and the details of the multiplexer are no need to show.

[Problem 3] 8-4-(-2)-(-1) is one 4-bit binary code that can be used to represent decimal digit, as listed in Table 1. Design a combinational circuit using minimum number of logic gates and literals that can check if the decimal input encoded by 8-4-(-2)-(-1) is a prime number, i.e., a positive integer that is greater than 1 and can be exactly divided by only 1 and itself. That is, the output f of the circuit equals 1 if and only if the decimal input is a prime number. You need to show the truth table of this circuit, the logic simplification process and the final logic diagram. Please note that the input code words (w, x, y, z) and their complements can be used directly as fan-in in the final logic diagram, and the unused input code words can be used as don't care conditions for logic simplification. (15%)

Table 1

Decimal digit	8-4-(-2)-(-1) code
0	0000
1	0111
2	0110
3	0101
4	0100
5	1011
6	1010
7	1001
8	1000
9	1111

[Problem 4] Implement the following Boolean function

$$F(x, y, z) = \sum(0, 1, 3, 5, 6)$$

(a) using only OR and inverter gates. (5%)
(b) using only NAND and inverter gates. (5%)
Please note that you only need to show the final Boolean function and how you derive the function.

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[Problem 5] A sequential circuit has three flip-flops *X*, *Y* and *Z*, a one-bit data input *I*, a one-bit clock input *CLK*; and a one-bit data output *O*. The state transition diagram of this circuit is shown in Figure 1. Please draw the logic diagram of this circuit using D flip-flops and minimum numbers of logic gates and literals. Please note that the details of the D flip-flop are no need to show, and the unused states can be used as don't care conditions for logic simplification. (15%)

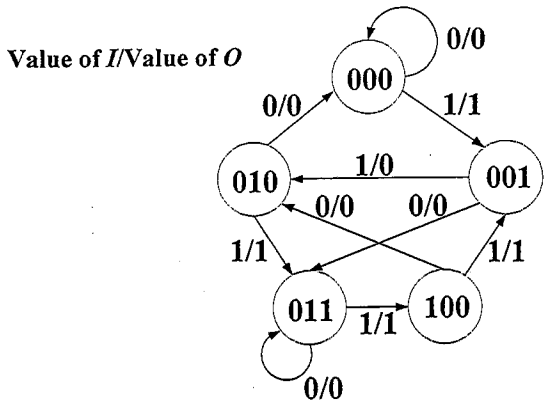

Figure 1

[Problem 6] Design an asynchronously resettable positive edge-triggered finite state machine that has a one-bit data input *x*, a one-bit clock input *clk*, a one-bit reset input *rst* and a one-bit data output *y*. The output is 1 only when an input sequence 110 or 101 appears. For example, the input sequence *x*=0110101010110 results in the output *y*=0001101010101.

(a) Draw the state transition diagram and define each state clearly. (10%)

(b) Write RTL Verilog/VHDL codes to implement the finite state machine you designed in (a). (10%)

[Problem 7] Please use four 1-bit full adder and a few logic gates (AND, OR, NOT, XOR) to design a 4-bit signed adder-subtractor. The details of the 1-bit adder are no need to show. This circuit can perform addition or subtraction operation, controlled by a mode input *M*. When *M*=0, the circuit performs addition (*A* + *B* where *A* and *B* are both 4-bit signed inputs, i.e., {A_3, A_2, A_1 and A_0} and {B_3, B_2, B_1 and B_0}), and when *M*=1, the circuit performs subtraction (*A* – *B*, i.e., *A* + the 2's complement of *B*). The outputs of this circuit include

(1) One 4-bit sum output *S* {S_3, S_2, S_1 and S_0}

(2) One 1-bit output *E* to indicate that the value of sum is odd or even: *E*=1(0) for even (odd) value

(3) One 1-bit output *P* to indicate that the parity of sum is odd or even: *P*=1(0) for even (odd) parity

(4) One 1-bit output *O* to indicate whether overflow occurs: *O*=1(0) means overflow happens (does not happen)

(5) One 1-bit carry-out output *C_out*. (15%)