國立中山大學101學年度碩士暨碩士專班招生考試試題

科目：計算機結構【電機系碩士班丙組、庚組】

題號：4069

[Problem 1] Terminology Explanation (20%)
(a) Multi-core Processor (b) Muti-threading (c) Parallel Processing
(d) Branch Prediction (e) Superscalar Processor

[Problem 2] (a) Describe the definition of Amdahl's law. (5%)
(b) Suppose we enhance a machine making all floating-point instructions run 10 times faster. If the execution time of some benchmark before the floating-point enhancement is 80 seconds, what will the speedup be if three-forth of the 80 seconds are spent executing floating-point instructions? (15 %)

[Problem 3] A set associative cache has a block size of four 32-bit words and a set size of 4. The cache can accommodate a total of 16K words. The main memory size that is cacheable is 1M * 32 bits. Design the cache structure and show how the processor's addresses are interpreted. (20%)

[Problem 4] Suppose we are considering a change to an instruction set. The base machine is a load-store machine. Measurements of the load-store machine showing the instruction mix and clock cycle counts per instructions are given in the following table:

Instruction Type	Frequency	Clock Cycle Count
ALU Operations	40%	1
Loads	20%	4
Stores	15%	4
Branches	25%	2

Let's assume that 25% of the ALU operations directly use a loaded operand that is not used again.

We propose adding ALU instructions that have one source operand in memory. These new register-memory instructions have a clock cycle count of 4. Suppose that the extended instruction set increases the clock cycle count for branches by 1, but it does not affect the clock cycle time. Would this change improve CPU performance? Explain your answer. (20%)

[Problem 5] (a) Briefly describe the Delayed branch scheme. (5%)
(b) Give three delayed-branch scheduling strategies and the requirement of each strategy. Also, describe situations in which the three strategies improve performance. (15%)