

本試題是否可以使用計算機： 可使用， 不可使用（請命題老師勾選）

考試日期：0301，節次：1

共九題(三頁)，請在答案卷作一表格如下，並清楚地填入這九個題目的答案，否則不予計分。  
請勿在本試題紙上作答，否則不予計分。

題號	答案
一	子題(1):
	子題(2):
	子題(3):
二	
三	子題(1):
	子題(2):
	子題(3):
四	
五	
六	子題(1):
	子題(2):
七	子題(1):
	子題(2):
八	
九	

一. [15%] Assume that the opcodes of the **add**, **addi** and **lw** instructions are respectively 000000, 001000 and 100011 in binary notation. Translate the following MIPS machine codes into corresponding assembly codes.

- (1) 00000001001010100100000000100000
- (2) 0010001011010101111111111001110
- (3) 10001101001010000000010010110000

二. [10%] Consider the assembly code as follows. Assume that the starting address of the first instruction is 10000 in the decimal notation. Translate the first and last instructions into corresponding machine codes, given that the opcodes of **beq** and **j** are 000100 and 000010 in binary notation.

```

Loop: beq    $9, $0, End
      add    $8, $8, $10
      addi   $9, $9, -1
      j     Loop
End:
    
```

三. [15%] Assume that a processor implements the hardware *TLB cache*. Assume also that the *instruction* and *data caches* are physical address caches. The processor includes the *write buffer* into its implementation.

(背面仍有題目,請繼續作答)

本試題是否可以使用計算機： 可使用， 不可使用（請命題老師勾選）

考試日期：0301，節次：1

- (1) For executing an instruction, what is the maximal number of cache misses that can be introduced to the processor? (need not consider the misses due to the exceptions handling)
- (2) What are these misses?
- (3) What is the function of the write buffer?

四. [10%] Consider a pipelined processor that executes the MIPS code shown in Figure 1 using the logic of hazard detection and data forwarding unit shown in Figure 2. If the MIPS code cannot be executed correctly, then how do we revise the logic shown in Figure 2 such that the code can be correctly executed?

```

add    $1, $1, $2
add    $1, $1, $3
add    $1, $1, $4

```

Figure 1: The MIPS code

```

if ( MEM/WB.RegWrite
    and ( MEM/WB.RegisterRd ≠ 0 )
    and ( MEM/WB.RegisterRd = ID/EX.RegisterRs ) )
then
    ForwardA = 01

if ( MEM/WB.RegWrite
    and ( MEM/WB.RegisterRd ≠ 0 )
    and ( MEM/WB.RegisterRd = ID/EX.RegisterRt ) )
then
    ForwardB = 01

```

Figure 2: The logic of hazard detection and data forwarding unit

五. [10%] Suppose a system contains 3 types of resources and 5 processes. The three types of resources X, Y and Z have 5, 2 and 7 instances, respectively. The snapshot of the system is as follows:

Process	Current Allocation			Maximum Demand		
	X	Y	Z	X	Y	Z
P0	1	1	1	3	1	1
P1	1	0	0	1	0	2
P2	0	0	1	1	1	2
P3	0	1	1	1	1	2
P4	3	0	2	4	1	3

本試題是否可以使用計算機： 可使用， 不可使用（請命題老師勾選）

考試日期：0301，節次：1

Answer the following question by using the banker's algorithm.

If a request from process 1 arrives for resource (0, 0, 1), can the request be granted immediately? Why or why not?

六. [10%] Consider the following hardware configurations.

Virtual address = 32 bits, page size = 4K bytes, and a page table entry occupies 4 bytes.

How many pages should the OS allocate for the page tables of a 12M-byte process under the following paging mechanisms?

- (1) [5%] one-level paging
- (2) [5%] two-level paging (assuming that the number of entries in a first-level page table is the same as that in a second-level page table)

七. [10%] Assume that a demand-paging system has 3 page frames, and the size of a page frame is 10 bytes. The memory is byte-addressable and the memory reference string is as follows:

Addresses: 70, 01, 12, 22, 01, 30, 02, 40, 22, 30, 02, 30, 22, 12

What are the page fault numbers under the following page replacement strategies?

- (1) [5%] Optimal
- (2) [5%] LRU

八. [10%] A file system uses a modified version of UNIX inodes. Each inode contains 10 direct entries, 2 single indirect entries and 1 double indirect entry. Assume that the size of a disk block is 1K bytes and the address of a block can be represented by 4 bytes. What is the maximum file size (in bytes) supported by the file system?

九. [10%] Four processes, W, X, Y and Z, arrive at a computer at time 2, 3, 0 and 5, respectively. The CPU burst time of them is listed in the following table. Assuming that the system only has a single processor (with a single core) and the context switch time can be ignored, please determine the average waiting time of the processes under the preemptive SJF scheduling algorithm.

Processes	Burst Time
W	4
X	2
Y	8
Z	7