1. Design a 64KB cache with different organizations and assume the cacheable memory size is 2GB. Answer the following questions;
   (a). The cache line size is 32 bytes and assume 8-way set associative cache mapping. What is the length of the (1) tag bits, (2) index bits, and (3) line size bits used respectively for the cache memory? 10%
   (b). The cache line size is 128 bytes and assume direct-mapped cache. What is the length of the (1) tag bits, (2) index bits, and (3) line size bits used respectively for this cache memory? 10%
   (c). If the cacheable memory size is 512MB, repeat (a) but for a fully set associative cache. 10%
   (d). Compute the total number of SRAM bits used for (a) for the entire cache assuming the cache uses write-back policy. This should include the total number of the tag bits, state bits, and data bits 10%

2. Design a single-cycle implementation of processor for the following MIPS-like instructions: lw Rt , offset (Rs), sw Rt, offset (Rs), add Rd, Rs, Rt, and beq Rs, Rt, label. Answer the following questions:
   (a). Show the datapath and control of this processor. 10%.
   (b). How to control the write for the data memory? Should it be edge-triggered or not? Why? 10%
   (c). Assume that the first step fetches an instruction from the memory using PC; also finally the PC is incremented by 4. Draw a relative timing diagram showing (1) at about what time, the PC+4 is valid, (2) at what time, the PC is updated, (3) at what time, the instruction fetched is obtained. State your assumptions. 10%

3. Convert the processor above (Problem 2) into a 5-stage pipelined processor. Answer the following questions:
   (a). Show the datapath and control of this processor. 10%.
   (b). Discuss how the processor handles control hazard for beq Rs, Rt, label. 10%
   (c). How to control the write for the data memory? Should this be edge-triggered or not? Why? 10%